**No. 22-1906**

**IN THE**

# United States Court of Appeals

**FOR THE FEDERAL CIRCUIT**

VLSI TECHNOLOGY LLC,

*Plaintiff-Appellee*,

v.

INTEL CORPORATION,

*Defendant-Appellant*.

On Appeal from the United States District Court
for the Western District of Texas
No. 6:21-cv-00057, Hon. Alan D. Albright

## NON-CONFIDENTIAL RESPONSE BRIEF OF APPELLEE VLSI TECHNOLOGY LLC

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## PATENT CLAIMS AT ISSUE

**Representative claim 9 of the ’373 Patent:**

An integrated circuit, comprising:

[a] a memory that operates using an operating voltage, wherein the memory is characterized as having a minimum operating voltage;

[b] a memory location that stores a value representative of the minimum operating voltage;

[c] a first voltage regulator for supplying a first regulated voltage;

[d] a circuit that provides a function and uses a first regulated voltage;

[e] a second voltage regulator for supplying a second regulated voltage, wherein the second regulated voltage is greater than the first regulated voltage; and

[f] a power supply selector that supplies the first regulated voltage as the operating voltage of the memory when the first regulated voltage is at least the minimum operating voltage and supplies the second regulated voltage as the operating voltage when the first regulated voltage is below the minimum operating voltage, wherein while the second regulated voltage is supplied as the operating voltage, the circuit uses the first regulated voltage.

Appx111 (13:7-28).

**Representative claim 14 of the ’759 Patent:**

A system, comprising:

[a] a bus capable of operation at a variable clock frequency;

[b] a first master device coupled to the bus, the first master device configured to provide a request to change a clock frequency of a high-speed clock in response to a predefined change in performance of the first master device, wherein the predefined change in performance is due to a loading of the first master device as measured within a time interval; and

[c] a programmable clock controller having an embedded computer program therein, the computer program including instructions to:

[d] receive the request provided by the first master device;

[e] provide the clock frequency of the high-speed clock as an output to control a clock frequency of a second master device coupled to the bus in response to receiving the request provided by the first master device; and

[f] provide the clock frequency of the high-speed clock as an output to control the variable clock frequency of the bus in response to receiving the request provided by the first master device.

Appx123-124(8:50-9:4).

# UNITED STATES COURT OF APPEALS
# FOR THE FEDERAL CIRCUIT

## CERTIFICATE OF INTEREST

**Case Number** 2022-1906

**Short Case Caption** VLSI Technology LLC v. Intel Corp.

**Filing Party/Entity** VLSI Technology LLC

**Instructions:** Complete each section of the form. In answering items 2 and 3, be specific as to which represented entities the answers apply; lack of specificity may result in non-compliance. **Please enter only one item per box; attach additional pages as needed and check the relevant box**. Counsel must immediately file an amended Certificate of Interest if information changes. Fed. Cir. R. 47.4(b).

I certify the following information and any attached sheets are accurate and complete to the best of my knowledge.

Date: 11/14/2022

Signature: /s/ Morgan Chu

Name: Morgan Chu

| **1. Represented Entities.** Fed. Cir. R. 47.4(a)(1). | **2. Real Party in Interest.** Fed. Cir. R. 47.4(a)(2). | **3. Parent Corporations and Stockholders.** Fed. Cir. R. 47.4(a)(3). |
|---|---|---|
| Provide the full names of all entities represented by undersigned counsel in this case. | Provide the full names of all real parties in interest for the entities. Do not list the real parties if they are the same as the entities.<br><br>☑ None/Not Applicable | Provide the full names of all parent corporations for the entities and all publicly held companies that own 10% or more stock in the entities.<br><br>☐ None/Not Applicable |
| VLSI Technology LLC | | CF VLSI Holdings LLC |
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☐ Additional pages attached

**4. Legal Representatives.** List all law firms, partners, and associates that (a) appeared for the entities in the originating court or agency or (b) are expected to appear in this court for the entities. Do not include those who have already entered an appearance in this court. Fed. Cir. R. 47.4(a)(4).

☐ None/Not Applicable ☑ Additional pages attached

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**5. Related Cases.** Provide the case titles and numbers of any case known to be pending in this court or any other court or agency that will directly affect or be directly affected by this court's decision in the pending appeal. Do not include the originating case number(s) for this case. Fed. Cir. R. 47.4(a)(5). See also Fed. Cir. R. 47.5(b).

☐ None/Not Applicable ☑ Additional pages attached

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**6. Organizational Victims and Bankruptcy Cases**. Provide any information required under Fed. R. App. P. 26.1(b) (organizational victims in criminal cases) and 26.1(c) (bankruptcy case debtors and trustees). Fed. Cir. R. 47.4(a)(6).

☑ None/Not Applicable ☐ Additional pages attached

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**Question 4. List all law firms, partners, and associates that (a) appeared for the entities in the originating court or agency or (b) are expected to appear in this court for the entities. Do not include those who have already entered an appearance in this court.**

IRELL & MANELLA LLP: Christopher Abernethy; Benjamin Manzin-Monnin; Iian Jablon; Jordan Nafekh; Keith Orso; Elizabeth C. Tuan; Ian Robert Washburn; Josh Gordon (*former*); Molly J. Russell (*former*); Michael Strub, Jr. (*former*); Brian M. Weissenberg (*former*)

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ROTHWELL FIGG ERNST & MANBECK, P.C.: Rachel Echols (*former*); Steven Lieberman (*former*); Daniel McCallum (*former*)

**Question 5. Related Cases. Provide the case titles and numbers of any case known to be pending in this court or any other court or agency that will directly affect or be directly affected by this court's decision in the pending appeal. Do not include the originating case number(s) for this case. Fed. Cir. R. 47.4(a)(5). See also Fed. Cir.R.47.5(b).**

- *VLSI Technology LLC v. Intel Corporation*, No. 1:19-cv-00977-ADA (W.D. Tex.) (formerly Nos. 6:19-cv-255-ADA, 6:19-cv-256-ADA)
- *VLSI Technology LLC v. Intel Corporation*, No. 6:21-cv-00299-ADA (W.D. Tex.) (formerly 6:19-cv-255-ADA)
- *VLSI Technology LLC v. Intel Corporation*, No. 1:18-cv-00966-CFC-CJB (D. Del.)
- *VLSI Technology LLC v. Intel Corporation*, No. 5:17-cv-05671-BLF (N.D. Cal.)
- *Intel Corporation v. Fortress Investment Group*, et al., No. 2021-0021-MTZ (Del. Ch.)
- *OpenSky Industries, LLC v. VLSI Technology LLC*, IPR2021-01064 (USPTO)
- *Patent Quality Assurance, LLC v. VLSI Technology LLC*, IPR2021-01229 (USPTO)
- *Intel Corp. v. VLSI Technology LLC*, IPR2022-00366 (USPTO)
- *Intel Corp. v. VLSI Technology LLC*, IPR2022-00479 (USPTO)
- *Patent Quality Assurance, LLC v. VLSI Technology LLC*, IPR2022-00480 (USPTO)
- *OpenSky Industries, LLC v. VLSI Technology LLC*, IPR2022-00645 (USPTO)

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**CONFIDENTIAL MATERIAL OMITTED**

Material has been redacted in the Non-Confidential Brief for Appellee VLSI Technology LLC. This material is confidential commercial information pursuant to the Confidentiality Order entered by the district court on September 16, 2019. Redacted material on pages 45, 46, and 53 contains confidential information regarding commercial patent-license royalties and sales volumes.

# TABLE OF AUTHORITIES

Page(s)

## CASES

**STATUTES**



**OTHER AUTHORITIES**

## STATEMENT OF RELATED CASES

Pursuant to Federal Circuit Rule 47.5, Appellee VLSI Technology LLC states:

a. This case was previously before this Court twice, in connection with mandamus petitions. *In re Intel Corp.*, 841 F. App'x 192 (Fed. Cir. 2020) (Prost, C.J., Lourie & Chen, JJ.); *In re Intel Corp.*, 843 F. App'x 272 (Fed. Cir. 2021) (Prost, C.J., Lourie & Chen, JJ.). This Court also previously dismissed Intel's appeals from PTAB decisions declining to institute IPR proceedings of VLSI patents, including the two patents at issue in this appeal. *Intel Corp. v. VLSI Technology LLC*, Nos. 21-1614, -1616, -1617, 2021 WL 5968443 (Fed. Cir. May 5, 2021) (Prost, C.J., O'Malley & Wallach, JJ.).

b. This Court's decision in this appeal may directly affect or be directly affected by the following pending cases: *VLSI Technology LLC v. Intel Corp.*, No. 1:19-cv-00977-ADA (W.D. Tex.) (formerly Nos. 6:19-cv-255-ADA, 6:19-cv-256-ADA); *VLSI Technology LLC v. Intel Corp.*, No. 6:21-cv-00299-ADA (W.D. Tex.) (formerly No. 6:19-cv-255-ADA); *VLSI Technology LLC v. Intel Corp.*, No. 1:18-cv-00966-CFC-CJB (D. Del.); *VLSI Technology LLC v. Intel Corp.*, No. 5:17-cv-05671-BLF (N.D. Cal.); *Intel Corp. v. Fortress Investment Group, et al.*, No. 2021-0021-MTZ (Del. Ch.); *OpenSky Industries, LLC v. VLSI Technology LLC*, IPR2021-01064 (USPTO); *Patent Quality Assurance, LLC v. VLSI Technology LLC*, IPR2021-01229 (USPTO); *Intel Corp. v. VLSI Technology LLC*, IPR2022-00366

(USPTO); *Intel Corp. v. VLSI Technology LLC*, IPR2022-00479 (USPTO); *Patent Quality Assurance, LLC v. VLSI Technology LLC*, IPR2022-00480 (USPTO); *OpenSky Industries, LLC v. VLSI Technology LLC*, IPR2022-00645 (USPTO).

## INTRODUCTION

Departing from the merits, Intel endeavors to portray VLSI as perpetrating a nefarious "scheme." Intel.Br.3. VLSI has merely sought fair compensation for Intel's infringement of intellectual property VLSI indisputably owns—valid patents for technologies developed by major semiconductor manufacturers that combined into NXP, which partnered with VLSI to enforce the patents. The scope of the verdict reflects the extent of Intel's pervasive infringement, using VLSI's patented technology in nearly a billion devices. On appeal, Intel raises five questions and myriad sub-issues. On inspection, Intel's arguments evaporate for each.

For example, Intel asserts that its products do not infringe the '373 patent because Intel's accused memory "operate[s] at a ***lower*** voltage than what VLSI's expert alleged was the '***minimum*** operating voltage.'" Intel.Br.3. The jury was entitled to reject that as sleight of hand: Intel compared devices at dramatically different temperatures—one at $\boldsymbol{0^0}$ and the other at $\boldsymbol{100^0}$. At the same temperature, the accused devices' RING_RETENTION_VOLTAGE ***is*** the claimed "minimum operating voltage." And Intel's reliance on prosecution history estoppel for the '759 patent conflates different amendments to different claim limitations for different purposes, as the district court found.

While Intel complains the jury saw Intel license agreements that "were ***not comparable*** to a hypothetical license to the asserted patents," Intel.Br.4, Intel never

mentions ***why*** those licenses were admitted. They were not used to calculate damages. They were admitted to rebut Intel's contention that VLSI's damages were not "in the same universe" with figures Intel would ***ever*** pay for a patent license in the "real world." The jury was entitled to hear "real world" evidence that debunked Intel's arguments. The Court should affirm.

## STATEMENT OF ISSUES

1. Whether substantial evidence, including Intel documents that contradict Intel's own expert's testimony, supports the jury's verdict that the accused devices literally infringe the asserted '373 patent claims.

2. Whether substantial evidence, including Intel's own documents, supports the jury's verdict that the accused devices infringe the asserted '759 patent claims under the doctrine of equivalents, and whether Intel's prosecution history estoppel argument fails because the patentee did not narrow the "master device" limitation to avoid prior art.

3. Whether the district court properly admitted nine- and ten-figure Intel patent licenses as rebuttal evidence, after Intel compared VLSI's damages to acquisition prices for professional sports franchises and suggested Intel would never pay similar sums for patent licenses.

4. Whether the district court properly admitted VLSI's damages theory, which calculated the apportioned technical and economic benefits of each patent, using Intel's own accused-product-specific tools and financial data.

5. Whether the district court acted within its discretion in rejecting Intel's untimely motion to add, sever, and stay a futile license defense, which Intel insisted the district court could not adjudicate in any event.

## STATEMENT OF THE CASE

### I. VLSI'S PATENTED TECHNOLOGY

This case involves VLSI's patented technology for improving microprocessor performance.

#### A. Technological Background

Modern processors include millions of circuits synchronized by a "clock." Appx1383-1384. Two key factors affect processors' power usage: frequency and voltage. Appx18109-18110(¶51); *see* Appx18089-18829. Frequency is the clock speed. Appx1384. Operating a clock at higher frequencies increases processor performance but uses more power. Appx1384-1386.

Voltage causes electrical current to flow in a circuit. A circuit may not work if voltage is too low. Appx1385-1386. The required voltage depends on factors like "type[] of circuitry" and variables like "temperature." Appx105; *see* Appx1384. It also depends on clock speed—higher frequencies require higher voltage. Appx1384-1385.

### B. VLSI's '373 Patent

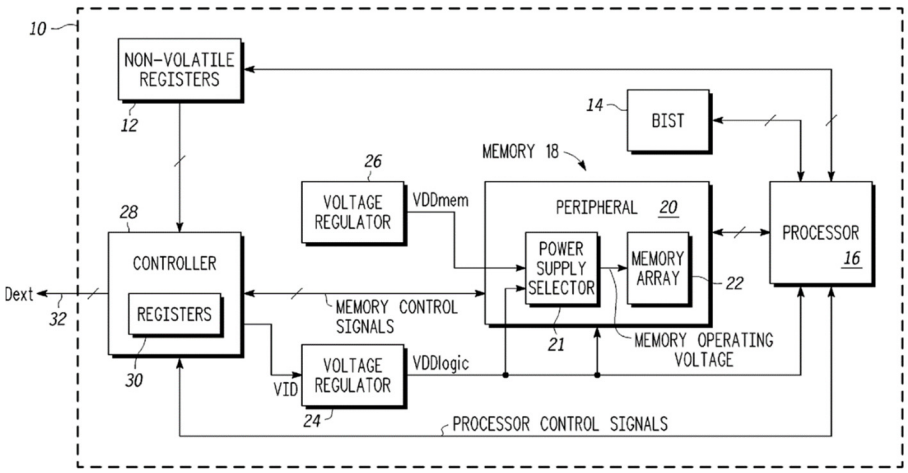
In 2006, David Bearden and a team of engineers at Freescale—a Motorola spin-off, Appx1332-1333; Appx1359; Appx1327-1328—were "working on a next-generation Freescale microprocessor." Appx1333. They understood that consumers wanted fast processors, but also "long[] battery life." Appx1329. To those ends, Bearden's team developed processors with "multiple operating states." Appx1335. They operated at full frequency and voltage when peak performance was required, but also could enter a "sleep" state to "save power." Appx1335-1337.

1. Bearden's team confronted a problem: Processors include logic circuits, which perform "calculations" or transfer data, and memory circuits, which "store data." Appx1335; Appx109(10:57-60). Those circuits have "different ranges of allowable operating voltages." Appx105(1:23-25). Voltage to logic circuits may be reduced when not performing calculations, but that voltage may be too low for memory circuits to retain data. Appx1336-1337; *see* Appx105.

Prior-art logic and memory circuits were "connected to a common power supply" and operated at the same voltage. Appx1336-1337. To avoid "los[ing] data," the entire processor's voltage needed to be sufficient for memory circuits—even when logic circuits were sleeping. Appx1336-1337; Appx1350-1351; Appx18112-18113(¶62).

2. Bearden's team solved that problem by developing a power-supply selector providing two separate power-supply pathways to memory, affording sufficient voltage to memory circuits while allowing voltage to logic circuits to drop below the threshold where memory experiences data loss. *See* Appx1341-1351. Freescale was granted the '373 patent for that invention. Appx101.[1]

As the figure below shows, logic circuits (16) are powered by a first voltage regulator (24) that supplies power at an adjustable voltage, "VDDlogic." Appx106(3:4-20). Controller (28) adjusts VDDlogic to achieve the desired frequency. *Id.* Memory (22) is connected to a power-supply selector (21). That selector can cause the memory to be powered ***either*** from the first voltage regulator, or a second voltage regulator (26) that supplies a voltage sufficient for the memory to operate, "VDDmem." Appx106.




[1] NXP merged with Freescale and partnered with VLSI to license the '373 patent. Appx1330; *see* Appx1272-1273.

Appx102.

The "controller indicates to [the] power supply selector which power supply to select." Appx107(5:42-45). When "VDDlogic remains above a minimum operating voltage," such as when processors are in high-performance states, the "power supply selector selects VDDlogic as the memory operating voltage." Appx106(3:30-35). "When VDDlogic is scaled below the minimum memory operating voltage," such as when processors enter low-power states, "the power supply selector selects the higher voltage, VDDmem" as the memory operating voltage. Appx106(3:35-38).

The "minimum operating voltage" need not be ***the*** minimum at which memory can ***ever*** work. Appx106(3:30-44, 4:12-16). There can be "one or more minimum operating voltages" for different operating states. Appx106(4:12-45). "[M]inimum operating voltage," moreover, "refers to a minimum which takes into consideration factors such as . . . temperature." Appx105(2:10-12). Thus, "the memory may actually be able to work at a voltage lower than the minimum voltage, depending on . . . temperature." Appx105(2:14-16).

3. Claim 9 of the '373 patent is representative:

An integrated circuit, comprising:

[a] a memory that operates using an operating voltage, wherein the memory is characterized as having a minimum operating voltage;

[b] a memory location that stores a value representative of the minimum operating voltage;

[c] a first voltage regulator for supplying a first regulated voltage;

[d] a circuit that provides a function and uses a first regulated voltage;

[e] a second voltage regulator for supplying a second regulated voltage, wherein the second regulated voltage is greater than the first regulated voltage; and

[f] a power supply selector that supplies the first regulated voltage as the operating voltage of the memory when the first regulated voltage is at least the minimum operating voltage and supplies the second regulated voltage as the operating voltage when the first regulated voltage is below the minimum operating voltage, wherein while the second regulated voltage is supplied as the operating voltage, the circuit uses the first regulated voltage.

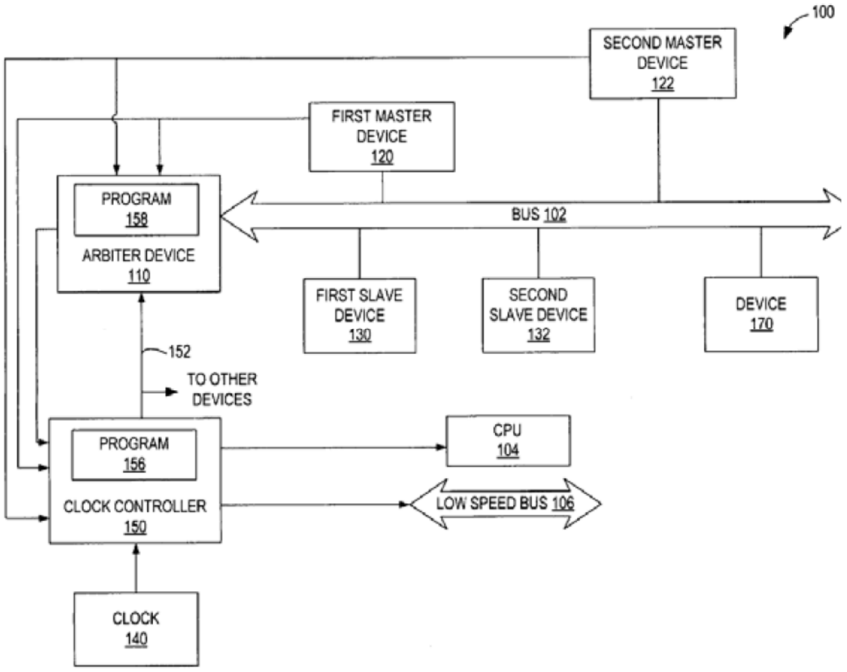
Appx111(13:7-28).

### C. VLSI's '759 Patent

At SigmaTel, Matthew Henson developed a processor that could "selectively deliver faster clock speeds" as needed, such as when users activate a device function, while otherwise running at lower frequency to save power. Appx120(1:23-25). "[C]onventional wisdom" was that computer ***operating systems*** should control processor frequency. Appx1413-1414. But Henson obtained dramatically better results by introducing a dedicated "microcontroller" to adjust frequency based on

user demand. Appx1415-1416. SigmaTel received the '759 patent for Henson's invention. Appx112.[2]

The '759 patent discloses "controlling a clock frequency" in a "system" that includes "a plurality of master devices," Appx120(1:45-50)—*i.e.*, "processor[s]," Appx120(3:23)—"coupled to a bus," Appx120(3:45-50). The system has a "programmable clock controller," App120(2:40-45), that controls the frequency of the system by setting the frequency of the bus, Appx121(3:39-51), and the frequency of the master devices, Appx122(5:29-35).




Appx114.

[2] SigmaTel was acquired by Freescale, which merged with NXP. Appx1278. NXP partnered with VLSI to enforce the '759 patent.

Based on workload monitoring, a master device sends the clock controller a "request for an increase to the clock frequency" when higher performance is required. Appx120(1:50-51); Appx121(4:5-10). The controller receives the request and uses that information to independently "control [the] clock frequency of [a] second master device" and the "bus." Appx121(4:43-50).

Claim 14 of the '759 patent is representative:

A system, comprising:

[a] a bus capable of operation at a variable clock frequency;

[b] a first master device coupled to the bus, the first master device configured to provide a request to change a clock frequency of a high-speed clock in response to a predefined change in performance of the first master device, wherein the predefined change in performance is due to a loading of the first master device as measured within a time interval; and

[c] a programmable clock controller having an embedded computer program therein, the computer program including instructions to:

[d] receive the request provided by the first master device;

[e] provide the clock frequency of the high-speed clock as an output to control a clock frequency of a second master device coupled to the bus in response to receiving the request provided by the first master device; and

[f] provide the clock frequency of the high-speed clock as an output to control the variable clock frequency of the bus in response to receiving the request provided by the first master device.

Appx123-124(8:50-9:4).

## II. PROCEDURAL HISTORY

In April 2019, VLSI sued Intel for infringing claims 1, 5, 6, 9, and 11 of the '373 patent, and claims 14, 17, 18, and 24 of the '759 patent. Appx74. After a trial, the jury found all asserted claims infringed, Appx9-10, and rejected Intel's validity challenges, Appx12. The jury awarded $2.175 billion in damages on nearly one billion infringing units. Appx13; Appx2575; Appx2796-2797.

### A. VLSI's Infringement Case

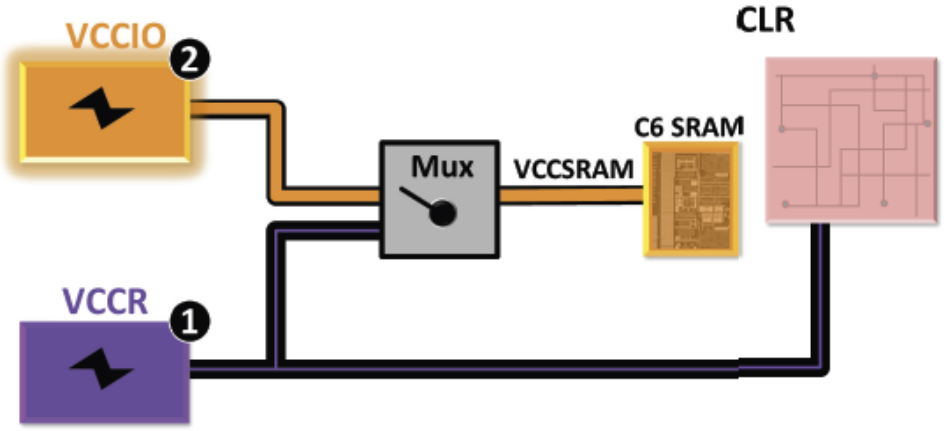
#### 1. *'373 Patent*

Intel's "Haswell" and "Broadwell" processors feature multiple "cores" that run computer programs. Appx1383. The cores are assisted by logic circuits—the "CBO," "LLC," and "Ring bus," collectively called the "CLR domain"—that provide data-transfer and caching functions. Appx3218-3219 (¶1280).

If all cores are idle, the processor can enter "deep sleep," called "PackageC7." Appx1388. In that mode, the CBO, LLC, and Ring circuitry can power off. Appx3225-3226 (¶¶1304-1305). The processor, however, must retain internal data so when the cores "wake up[,] they can pick up where they left off." Appx1395. That data is stored in memory called "C6SRAM." *Id.*

Intel's processors contain two voltage regulators, which Intel calls VCCR and VCCIO. Appx2656. VCCR supplies power to the CLR domain at an adjustable voltage. Appx2656-2658; Appx15057. VCCIO supplies power at a fixed voltage to components that "interface to external devices." Appx2660. The C6SRAM is

connected to both VCCR and VCCIO by a selector called a "power supply mux." Appx2664.




Appx15063.

Ordinarily, VCCR supplies the CLR domain and C6SRAM. Appx2664. VCCR may be adjusted based on frequency but usually remains above a minimum operating voltage, RING_RETENTION_VOLTAGE. Appx2667. That "defines the worst case ***retention voltage***"—*i.e.*, "the lowest voltage for memory to still remember." Appx2656-2657. Intel stores that voltage in non-volatile memory called "fuses." Appx2655-2656; Appx15098. The stored value is for 0° C, and an "inverse temperature dependence" adjustment accounts for actual processor temperature. Appx2730.

In PackageC7 mode, the CBO, LLC, and Ring are "put to sleep," and VCCR is reduced below RING_RETENTION_VOLTAGE. Appx2666. When that happens, "the [power supply] mux is switched" so that the C6SRAM is powered by VCCIO, "which never powers down." *Id.*

VLSI's expert Dr. Conte testified that the accused devices meet every claim limitation. Appx2674. VCCR is the "first regulated voltage" [c], and the CBO, LLC, and Ring are the logic "circuit[s]" that "use[ ] the first regulated voltage" [d]. Appx2661-2662. VCCIO is the "second regulated voltage," which is "greater than the first regulated voltage" when VCCR powers down [e]. Appx2663. The power supply "mux" corresponds to the "power supply selector" [f]. Appx2664.

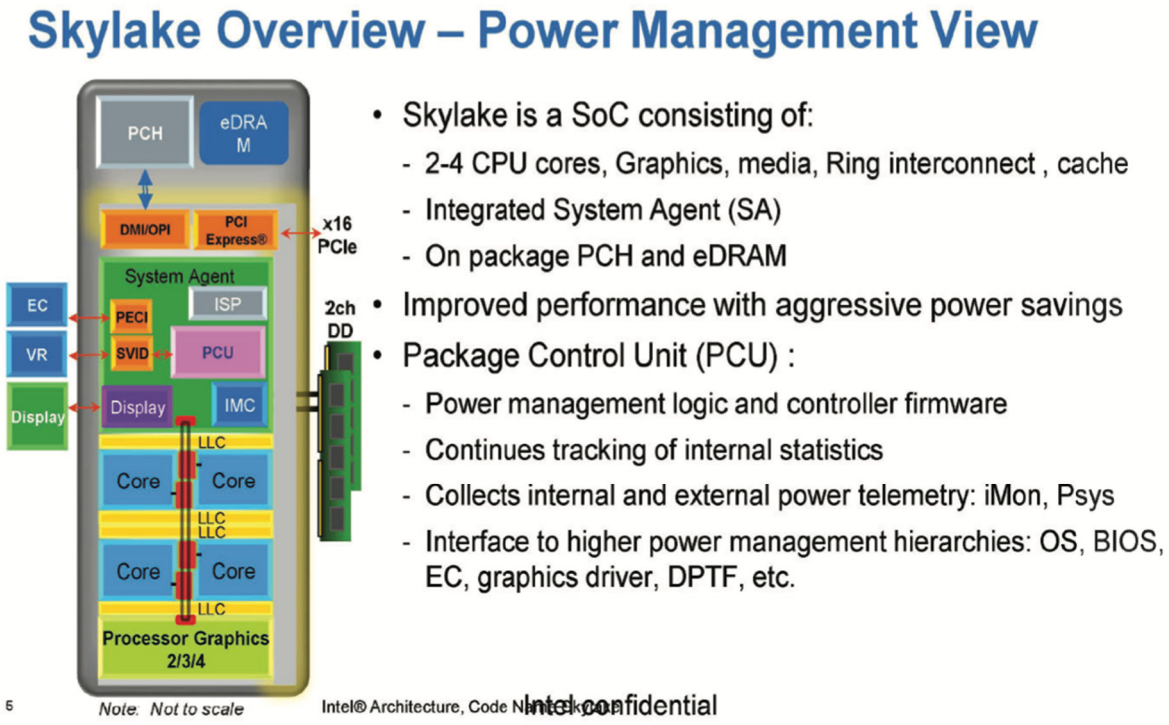
When VCCR remains higher than the RING_RETENTION_VOLTAGE (minimum operating voltage [a]), the mux supplies VCCR (the first regulated voltage) to the CLR domain and the C6SRAM. Appx2665-2666. But when the processor enters PackageC7, VCCR is reduced below RING_RETENTION_VOLTAGE, and the mux switches to supplying the C6SRAM through VCCIO (the second regulated voltage). *Id.*

Intel's expert, Dr. Sylvester, asserted that RING_RETENTION_VOLTAGE cannot be the recited "minimum operating voltage" because the C6SRAM can operate at a ***lower*** voltage, RING_VF_VOLTAGE_0. Appx1852; Appx1949-1950; Appx15339. Conte explained that was a false comparison. Appx2427-2429. Sylvester used RING_VF_VOLTAGE_0 at ***100°*** C, compared to RING_RETENTION_VOLTAGE at ***0°*** C. "[C]alibrated to the same temperature," RING_RETENTION_VOLTAGE is always ***lower*** than RING_VF_VOLTAGE_0

and thus is the "minimum" for any temperature—as Intel's own documents established. Appx2429-2430. The jury credited Conte, finding infringement. Appx9.

2. *'759 Patent*

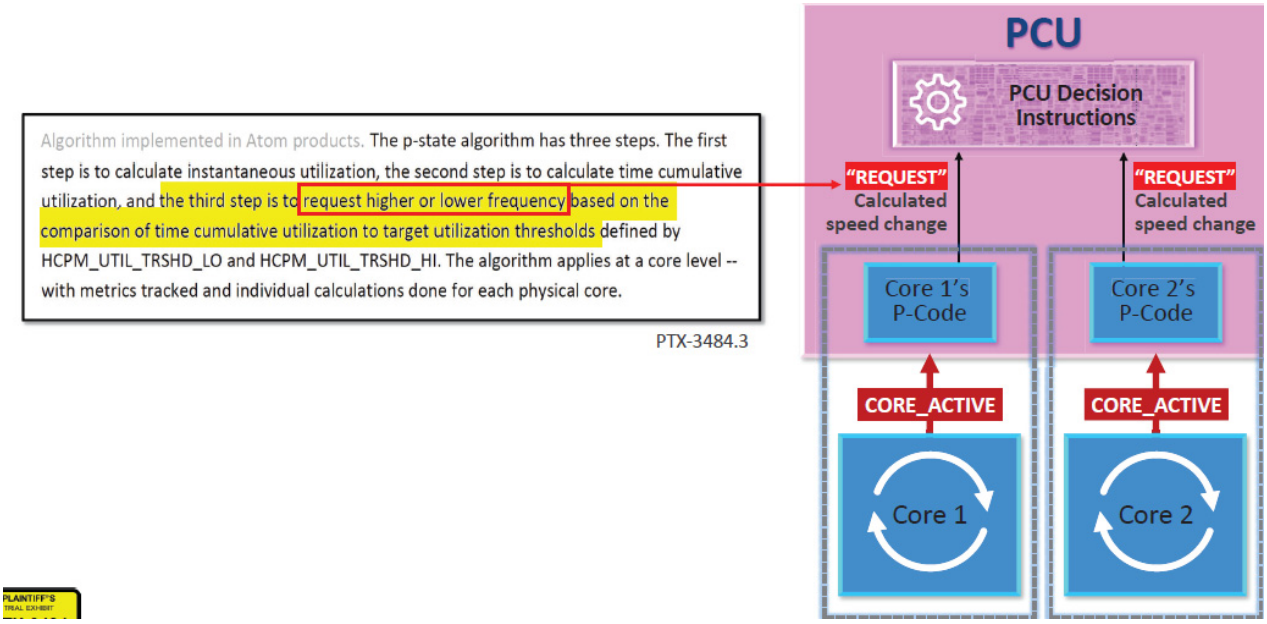
VLSI accused Intel's "Lake" processors, and their "SpeedShift" feature, of infringing the '759 patent. Those processors have cores, and a "Ring" bus connecting the cores. Appx2688-2689. They also have a "power control unit" ("PCU")—a microcontroller running programs called "P-code"—that controls the frequency of the cores and Ring bus. Appx2696-2697; *see* Appx15181-15188; Appx19340.




Appx15129.

Each core monitors and reports its workload by enabling a "Core_Active" signal. Appx2690-2692. Core-specific P-code in the PCU receives that signal,

"calculates a requested speed change" as necessary, and sends it to different P-code (the "decision instructions"). Appx2706-2708. That module receives the speed-change request and adjusts a second core's clock frequency and the ring bus's clock frequency based on performance requirements and the processor's "power budget." Appx2702; Appx2707-2710.




Appx15183.

Conte testified that SpeedShift infringes the '759 patent under the doctrine of equivalents. Appx2690-2705; Appx2713. The PCU's "decision instructions" module running on the microcontroller is the claimed "programmable clock controller." Appx2706-2708. The core, together with the core-specific P-code, is equivalent to the claimed "master device." That combination performs the same "function" of providing the claimed "request" to change clock frequency; it performs the function

the same way, monitoring processor "load" (through the CORE_ACTIVE signal); and produces the same result, the literal "request." Appx2706-2707. Intel's expert, Dr. Grunwald, presented no currently relevant substantive response to Conte's equivalents theory. Appx2200-2201. The jury found infringement. Appx10.

**B. Damages Evidence**

1. VLSI calculated reasonable royalties based on the incremental value its patented technology added to Intel's infringing devices.

'373 Patent. Drs. Conte and Annavaram used Intel's proprietary, accused-product-specific "Power Models," Appx3143-3146(¶¶96-104), Appx19454-19474, to compare the infringing technology with the closest non-infringing alternative, finding the patent saves at least 5.45% power in the accused products, Appx2681-2683; Appx1527-1540.

'759 Patent. Conte began with Intel's own performance-test data comparing SpeedShift to a non-infringing design. Appx2718-2725. After additional apportionment using another accused-product-specific "Fox2" simulator, Conte found the patent increased the accused processors' performance by 1.11%. Appx123-124; Appx2722-2723; Appx15211-15214, Appx3210-3216(¶¶1236-1254).

2. Dr. Sullivan then calculated the performance benefits' economic value. Given the well-known "tradeoff" between power and frequency, Intel could use the inventions to "reduce power" or "increase clock speed," and Sullivan could

analyze the inventions' benefits in terms of "improvement in clock speed." Appx1606-1607; Appx2455-2457; Appx3285-3302(¶¶1699-1725); Appx3364-3379(¶¶54-67); Appx15105-15107; Appx15215. Using regression, Sullivan quantified the relationship between speed and price. Appx1605-1622; Appx15276-15278; Appx3414-3438(¶¶166-197).

Applying the patents' incremental speed benefits with the speed-price relationship and accused revenues, Sullivan computed Intel's infringement-specific revenues from "use of [VLSI's] technology." Appx1654-1664; Appx3446-3448(¶¶219-233). Sullivan then calculated incremental profits and apportioned them between the parties based on their "relative contributions" to arrive at reasonable royalties of $1,611,609,964 and $831,863,261, respectively. Appx1599-1664; Appx3452-3453(¶¶240-245); Appx3461-3474; Appx15297-15306.

3. Intel's expert, Mr. Huston, presented a comparable-license analysis based on certain Intel "microprocessor patent" agreements. Appx2776. Huston estimated a $2.2 million lump-sum royalty based on an alleged "going rate" for "microprocessor patents," Appx2779-2780; Appx15403-15409, disregarding the number of infringing units, Appx2795-2797.

Intel offered minimal expert rebuttal to Sullivan's analysis. Intel's counsel mainly portrayed VLSI's damages numbers as outside the "real-world" "universe" of patent licenses, Appx2611, comparing them to the $1.5 billion acquisition of the

"Dallas Mavericks," and the "astronomical" prices of the "Atlanta Hawks" and "LA Clippers." Appx1700-1701. In rebuttal, VLSI showed that Intel had paid similar prices for microprocessor patent licenses. Appx2801-2806; Appx2501-2507.

### C. The District Court Denies Intel's Post-Trial Motions and Motion To Amend

Intel filed numerous post-trial motions, which the district court denied in thorough opinions.

#### 1. *Intel's Rule 50(b) Motion on Infringement*

The district court denied Intel's motion for JMOL of non-infringement, finding substantial evidence supported the verdict.

'373 Patent. The court rejected Intel's argument that RING_RETENTION_VOLTAGE was not the claimed "minimum operating voltage." Appx77. Intel urged C6SRAM would operate at RING_VF_VOLTAGE_0, and insisted that was a lower voltage. But the jury was entitled to credit Conte's testimony, based on Intel documents, that RING_VF_VOLTAGE_0 was higher at any particular temperature. Appx78; *see* Appx1425-1426; Appx1451-1452.

The court rejected Intel's argument that "VLSI introduced no evidence that the RING_RETENTION_VOLTAGE fuse value is ever used to guide 'when' VCCR and VCCIO are supplied." Appx80. Conte demonstrated, using "Intel documents," that "RING_RETENTION_VOLTAGE acts as the threshold for when"

VCCR or VCCIO are supplied to the C6SRAM. Appx81. The court declined Intel's invitation to "[re]weigh[ ] the evidence." *Id.*

'759 Patent. The court found substantial evidence supporting the jury's finding that Intel infringed under the doctrine of equivalents. Appx84. Intel contended that Conte identified the same component, the PCU, as both "send[ing] and receiv[ing] the claimed 'request' [to increase frequency]." Appx87. As the court explained, however, Conte distinguished between the master device ("'the core and [core-specific] P-Code'") and the programmable clock controller (the "'PCU decision instructions'"). *Id.* The court also found that, insofar as Intel argued that the master device and programmable clock controller "must always comprise entirely separate and distinct circuits," that "new claim construction" argument was "waived." *Id.*

2. *Intel's Rule 52 Motion of Non-Infringement of the '759 Patent*

Intel sought judgment of non-infringement for the '759 patent based on prosecution history estoppel (and other now-abandoned theories). Appx23. The court rejected Intel's challenges. Appx23-64. According to Intel, a 2008 amendment required the "request" to change clock frequency to be made by "only one master device"—supposedly excluding VLSI's theory that a core and the core-specific P-code together comprise the "master device." Appx51.

| **Rejected Claim 22** | **Asserted Claim 14** |
|---|---|
| ***at least one*** master device coupled to the bus, … wherein ***the at least one*** master device provides a corresponding trigger input, wherein the trigger input includes a request to change the variable clock frequency | ***a*** first master device coupled to the bus, ***the*** first master device configured to provide a request to change a clock frequency of a highspeed clock in response to a predefined change in performance of ***the*** first master device |

Appx50.

The court found the "amendment did not cause a substantive change in the claim language" because, under black-letter patent law, "a" means "one or more." Appx52. The court found nothing suggesting the amendment limited claims to "only one master device making the request." Appx33. Intel erroneously asserted that the "master device" amendment was designed to overcome a rejection based on Ansari. Appx53-55. The patentee had amended ***other*** limitations to overcome Ansari. *Id.* But "[n]othing in the Applicant's argument" to the examiner "disclaimed" VLSI's DOE theory—"that the core and its associated P-code in the PCU could provide the request." Appx55.

3. *Intel's Rule 50(b) and Rule 59 Motions on Damages*

The district court denied Intel's motions for JMOL or a new damages trial.

The court rejected Intel's assertion that it erred by admitting Intel license agreements that responded to "discrepancies" in Intel's damages themes and testimony. Appx17-18. Intel's contention that the licenses implied "past wrong-doing" was "unpersuasive." Appx18.

The court rejected Intel's *Daubert* arguments, including that "VLSI's damages opinion included improper technical inputs." Appx19. And arguments about "Sullivan's inclusion of non-accused products and features" were "properly addressed to the model's weight, not admissibility." *Id.*

The court rejected Intel's argument that "no reasonable jury could value the asserted patents at $2.175 billion," as the jury "considered evidence presented by both parties," including evidence that "Intel made over $3 billion [in additional revenues] from the nearly one billion [infringing] products it sold." Appx95-96. The court had already rejected Intel's *Daubert* arguments, and Intel offered "no additional compelling reasons" for reconsideration on JMOL. Appx96.

4. *Intel's Motion To Amend, Sever, and Stay*

Months after having all necessary knowledge, after discovery closed, and just weeks before the scheduled trial, Intel filed a motion to amend its answer to add a license defense. Intel's motion urged the district court to "sever and stay" the defense, arguing it could be adjudicated only in Delaware Chancery Court. *E.g.*, Appx3636-3637 & n.2.

Denying the motion, the court found Intel had "inexcusab[ly]" waited three months after learning the underlying facts before seeking to amend, and that the "late filing of its Motion resembles more of a tactic to delay trial rather than a good faith basis for adding its defense." Appx68. The court found the amendment would be

futile, as VLSI was neither party to the license agreement nor bound by its terms. Appx68-71. And Intel's request to sever and stay was moot, as the Chancery Court had dismissed Intel's complaint before the district court ruled. Appx72.

## SUMMARY OF ARGUMENT

**I.** Substantial evidence supports the jury's conclusion that the '373 patent's "minimum operating voltage" limitation covers the accused products' RING_RETENTION_VOLTAGE, which Intel's documents call the "worst case retention voltage" for the C6SRAM. The jury was not required to believe Intel's theory that the minimum voltage is RING_VF_VOLTAGE_0, based on a made-for-litigation comparison that failed to correct for inverse temperature dependence, improperly comparing those voltages at different temperatures.

Substantial evidence supports the jury's conclusion that the accused products' "mux" supplies the first or second regulated voltage "when" the patent's claims require. Intel urges that the mux does not "use" the minimum operating voltage in making the switching decision. But the claims are phrased in terms of "when" the first or second voltage is supplied; they do not require some unspecified "use" of the minimum operating voltage.

**II.** Substantial evidence supports the jury's conclusion that Intel infringes the '759 patent under the DOE. It is undisputed that the combination of an Intel "core" and its core-specific "P-code" "provide" the claimed "request to change a

clock frequency." The fact that the P-code is located in the PCU does not defeat infringement.

The district court properly rejected Intel's prosecution history estoppel argument. The patentee's amendments to the "master device" limitation did not narrow claim scope. Intel's argument that the amendment was made to distinguish the Ansari reference misreads the prosecution history.

**III.** The district court properly admitted the Intel licenses as rebuttal evidence. It admitted them only after Intel denigrated VLSI's damages as inconsistent with "real-world" Intel licenses for "microprocessor patents," and drew irrelevant comparisons to sports-team acquisitions when cross-examining VLSI's damages expert. Intel also shows no prejudice. VLSI acknowledged it was not offering the licenses as comparable, and the jury was instructed that non-comparable licenses could not be used in determining damages.

**IV.** VLSI's damages evidence was properly admitted. VLSI's experts quantified the technical benefits of VLSI's patents; computed the economic value of those benefits using standard regression analysis; estimated Intel's incremental revenues and profits based on that economic value; and allocated that profit between Freescale/VLSI and Intel based on Intel's "contributions" to commercializing VLSI's technology. Contrary to Intel's argument, non-infringing features were regression variables to be properly ***factored out*** to "isolate" the patents' value. Intel

raises no substantial challenge to how VLSI's experts calculated technical benefits by comparing against non-infringing alternatives. It quibbles about the results of ancillary testing that never entered the benefits calculations. Those arguments—which Intel made to the jury—lack merit. Intel identifies no abuse of discretion requiring exclusion of VLSI's damages case.

**V.** The district court did not abuse its discretion in denying Intel's motion to amend, sever, and stay. The court reasonably found Intel's motion untimely and tactical, as Intel waited ***months***, until discovery deadlines had passed and the eve of trial arrived, to seek to amend. The court also properly found Intel's purported license defense was futile, as Intel failed to show how a 2012 settlement between ***Intel*** and ***Finjan*** could vitiate ***VLSI's*** patent rights. Nor did Intel seek to adjudicate the defense in this case, instead contending that the issue had to be resolved in Chancery Court.

## ARGUMENT

### I. SUBSTANTIAL EVIDENCE, INCLUDING INTEL'S OWN DOCUMENTS, SUPPORTS THE JURY'S VERDICT THAT INTEL INFRINGES THE '373 PATENT

Seeking to overcome the jury's verdict that Intel infringes the '373 patent, Intel urges VLSI did not prove that the accused Haswell and Broadwell processors (1) "store the claimed 'minimum operating voltage,'" Intel.Br.26; and (2) "provide the first and second regulated voltages 'when' the claims require," Intel.Br.33. Intel does not remotely show that no "reasonable jury, given the record before it viewed

as a whole, could have" found infringement. *Broadcom Corp. v. Qualcomm Inc.*, 543 F.3d 683, 696 (Fed. Cir. 2008).

### A. Substantial Evidence Supports the Jury's Finding Regarding the "Minimum Operating Voltage" Limitation

The claims recite memory, and "stor[ing] a value representative of the minimum operating voltage" of that memory. Appx111 (13:60-63). VLSI presented evidence that Intel's products store precisely that value. Dr. Conte explained that a fuse in the units labeled RING_RETENTION_VOLTAGE stores the minimum voltage at which memory—the C6SRAM—can retain data. Appx2655-2657. According to ***Intel's*** documents, RING_RETENTION_VOLTAGE "***defines the worst case retention voltage for [the] RING [domain]***," which includes the C6SRAM. Appx9574 (emphasis added); Appx12642. Conte analyzed Intel's products, source code, and documentation and confirmed that RING_RETENTION_VOLTAGE corresponds to a minimum retention voltage (the recited "minimum operating voltage") for the C6SRAM. Appx2655-2659.

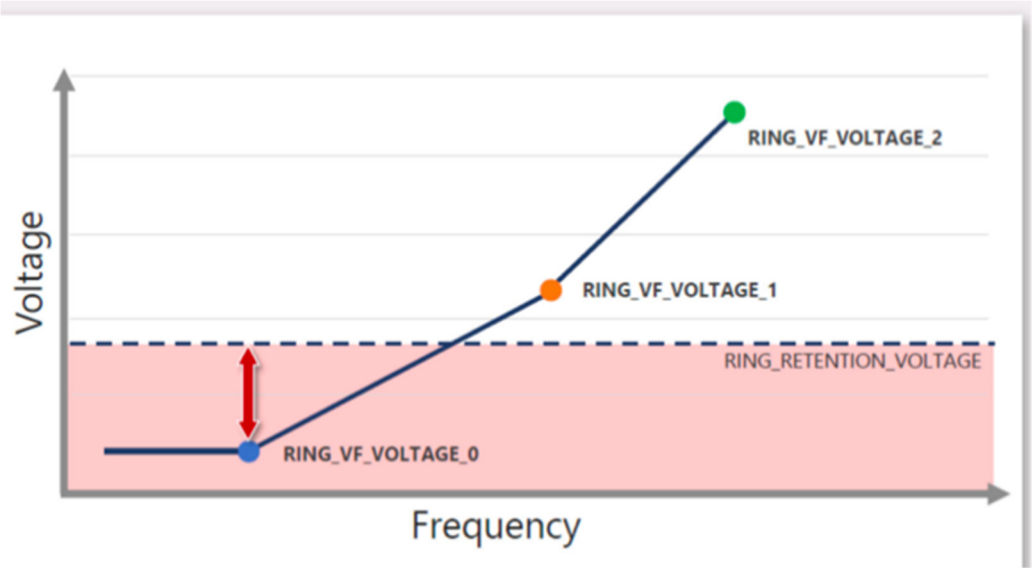
1. Unable to dispute its own documents, Intel attempts to distinguish "the entire ring domain" from C6SRAM. Intel.Br.32. VLSI, it says, was "required to prove that RING_RETENTION_VOLTAGE is a 'minimum operating voltage' ***of the C6SRAM***, not of some larger collection of components." *Id.* But the jury credited Conte's explanation that "***retention*** voltage" applies only to "memory," and that the only other memory in the RING domain is made of "identical bit cell

circuitry" as the C6SRAM. Appx2424 (emphasis added); *see* Appx3236. That makes sense: It is memory that engages in "retention" of data. The jury reasonably credited Conte's testimony that the "worst case retention voltage for [the] RING [domain]" is the same as the worst case retention voltage for the C6SRAM. Appx3267.

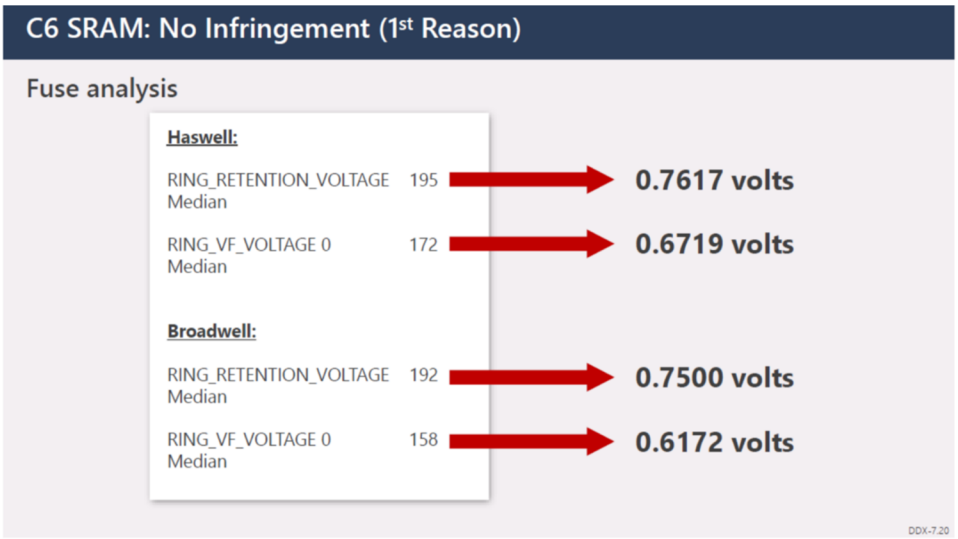
Intel's expert never testified otherwise. And other Intel documents further confirm Conte's testimony. The RING_RETENTION_VOLTAGE in samples of accused devices was ~0.75 volts. Intel.Br.28-29. That corresponds to the "0.75 [volts]" that Intel documents describe as "Vmin for [the] C6SRAM"—which Intel's expert acknowledged refers to a "minimum voltage." Appx1946; *see* Appx1985-1987; Appx3235.

2. Intel argues that RING_RETENTION_VOLTAGE is not the re-cited "***minimum*** operating voltage," because "RING_VF_VOLTAGE_0 . . . is ***lower*** than RING_RETENTION_VOLTAGE," and "C6SRAM is 'fully operational' and retains data at" RING_VF_VOLTAGE_0. Intel.Br.29-30. The jury rejected that argument, with reason: Intel compares RING_RETENTION_VOLTAGE at one temperature, with RING_VF_VOLTAGE_0 at a different temperature. When compared at the same temperature, RING_RETENTION_VOLTAGE is always lower.

Intel's expert Dr. Sylvester testified that the operating voltage value for the RING_VF_VOLTAGE_0 fuse is "significantly lower" than RING_RETENTION_VOLTAGE, Appx1950, using made-for-litigation demonstratives:




Appx15343.



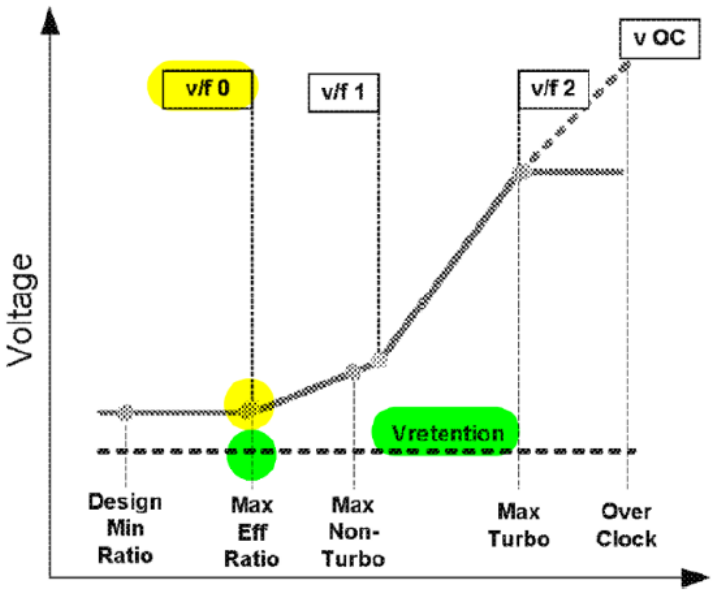

Appx15342.

Conte explained that Sylvester's testimony did not reflect an "apples-to-apples" comparison. Appx2430. Conte testified that, due to "inverse temperature dependence," a memory's retention voltage is affected by temperature. Appx2427. Thus, any meaningful comparison of minimum operating voltages must "compensate for" differences in the temperature at which those voltages are measured. Appx2429.

Sylvester did not do that. In his comparison, RING_VF_VOLTAGE_0 "is measured at ***100 degrees*** Celsius," while "RING_RETENTION_VOLTAGE is measured at ***zero degrees*** Celsius." Appx2429 (emphases added). Consequently, Sylvester's comparison did not show that RING_VF_VOLTAGE_0 is ***ever*** lower than RING_RETENTION_VOLTAGE ***under comparable conditions***. *Id.* Intel invokes its "engineers[']" testimony, Intel.Br.27-28, but cites only Sylvester's debunked demonstratives, Appx15343, Appx15322; testimony from an engineer who made the same misleading comparison, Appx1854-1855, Appx1859-1861; and testimony from an engineer who never compared RING_RETENTION_VOLTAGE with RING_VF_VOLTAGE_0 at all, Appx2757-2760 (discussing Appx14252-14280). Intel never presented apples-to-apples, ***temperature-corrected comparisons*** to support its theory.

Intel asserts Conte "never performed any calculations" to show how the values of RING_VF_VOLTAGE_0 "should have been adjusted." Intel.Br.30. But VLSI

was not required to ***correct*** defects in ***Intel's*** argument; proving it lacked credibility sufficed. And Conte ***did*** directly refute Intel's theory. Using an ***Intel*** technical manual, he showed that, "[w]hen you compensate for temperature," RING_VF_VOLTAGE_0 "is going to be always above the RING_RETENTION_VOLTAGE." Appx2430. The manual included a voltage-versus-frequency chart for the accused products showing that "Vretention," which Conte explained corresponds to RING_RETENTION_VOLTAGE, is ***lower*** than "v/f 0," which he explained corresponds to RING_VF_VOLTAGE_0. Appx2425-2426; Appx2430-2431.




Appx19243.

Intel quibbles that the document "describes a generic voltage at which data retention occurs," and does not use the term RING_RETENTION_VOLTAGE.

Intel.Br.31. Intel also argues that its expert interpreted "Vmin" as something other than a "minimum operating voltage." *Id.* But a reasonable jury could credit Conte's explanation of the document's technical terms. Appx2430-2431. And although Intel complains that the document was a "draft specification," Intel.Br.31, it never identified a different version of the document.

3. Intel's theory that VLSI must prove RING_RETENTION_VOLTAGE "is ***literally*** the '***minimum*** retention voltage'" for the C6SRAM, regardless of conditions, Intel.Br.30, fails three times over. First, if the claims required that, a reasonable jury could find that ***Intel's*** documents, which describe RING_RETENTION_VOLTAGE as the "***worst case*** retention voltage," suffice. Appx9574 (emphasis added).

Second, Intel never sought a claim construction defining "minimum operating voltage" as the minimum possible voltage, irrespective of conditions. Absent such a construction, the jury could reasonably understand the minimum operating voltage as the minimum for a given set of conditions (*e.g.*, for a particular temperature). *See Avid Tech., Inc. v. Harmonic, Inc.*, 812 F.3d 1040, 1048 (Fed. Cir. 2016) (court must defer to jury's understanding of "un-construed" limitation unless it defies "the only reasonable view" of the limitation). The contrary view would defeat the invention: Setting the voltage at the minimum potential voltage for ***any*** condition would result in data loss when conditions are less optimal (*e.g.*, higher temperatures). *See AIA*

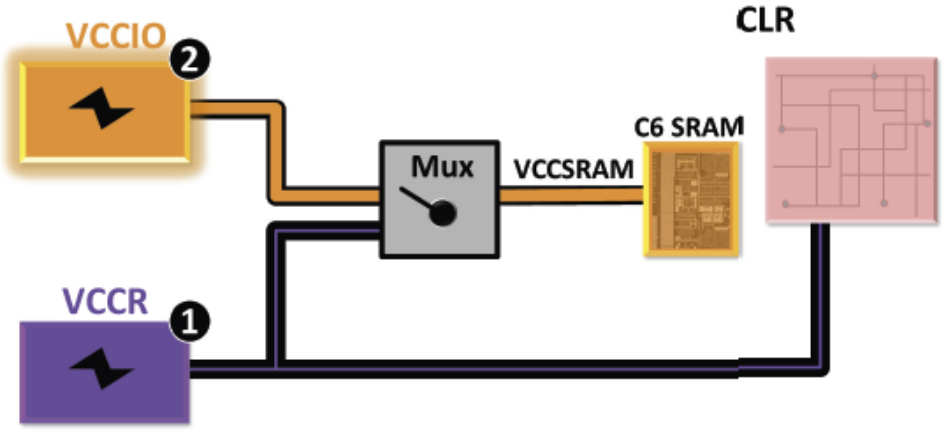
*Eng'g Ltd. v. Magotteaux Int'l S.A.*, 657 F.3d 1264, 1278 (Fed. Cir. 2011) ("extreme skepticism" for "construction that renders the claimed invention inoperable").

Third, the specification refutes Intel's argument. Appx107(6:25-26). The specification says, "as used herein, the minimum voltage or minimum operating voltage refers to a minimum which takes into consideration factors such as, for example, temperature." Appx105(2:9-13). Thus, "there may be situations where the memory may actually be able to work at a voltage ***lower than the minimum voltage*** depending on . . . factors such as temperature." Appx105(2:12-16) (emphasis added). The accused devices operate in precisely that way, storing a "minimum" voltage that is then adjusted based on factors like temperature. Intel cannot avoid infringement through sleight-of-hand, comparing RING_VF_VOLTAGE_0 at one temperature and RING_RETENTION_VOLTAGE at another.

### B. Substantial Evidence Supports the Jury's Finding that the Accused Products Supply First and Second Voltages "When" Required

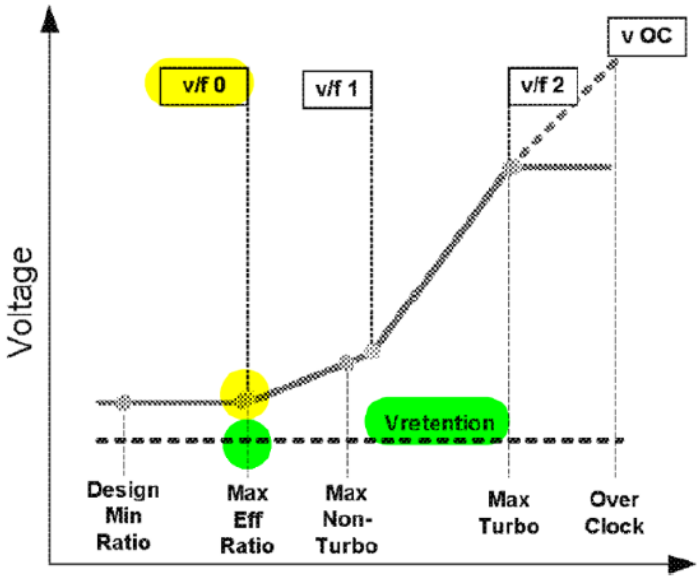
Representative claim 9 recites "a power supply selector that supplies the first regulated voltage" to memory "when the first regulated voltage is at least the minimum operating voltage," and "the second regulated voltage" to memory "when the first regulated voltage is below the minimum operating voltage." Appx111(14:8-13). Substantial evidence shows Intel's products "provide the first and second regulated voltages" "when" the claims require. Intel.Br.33.

1. Conte identified the Intel processors' "VCCR" as the first regulated voltage, and "VCCIO" as the second regulated voltage. *See* pp. 11-12, *supra*.




Appx15063. He testified that RING_RETENTION_VOLTAGE, ~0.75 volts in the accused products, is the C6SRAM's minimum operating voltage. *See* pp. 11-12, *supra*. And, Conte explained, those products contain a "power supply mux" that supplies either VCCR or VCCIO to the C6SRAM, switching from VCCR (the first regulated voltage) to VCCIO (the second regulated voltage) when the former drops below the minimum operating voltage. Appx2664-2670.

VCCR is set based on a "VF curve," which "determine[s] what voltage [the processor] needs to use for a given frequency." Appx2757-2758. The VF curve specifies a VCCR voltage ***above*** RING_RETENTION_VOLTAGE while the processor is active. Appx2430-2431; *see* Appx2665. Intel's documents thus depict a VF curve where the voltages are all above "Vretention," which Conte testified refers to RING_RETENTION_VOLTAGE:




Appx19243; Appx2425-2426; Appx2430-2431. Conte explained that, in other active modes, VCCR can drop "down to RING_RETENTION_VOLTAGE"—but no lower. Appx2667-2668. During these times when VCCR is ***at least*** RING_RETENTION_VOLTAGE—when the processor is actively operating or sleeping lightly—the mux supplies the VCCR voltage to the C6SRAM. Appx2664. Thus, "when" VCCR is "at least the minimum operating voltage" of RING_RETENTION_VOLTAGE, "the first regulated voltage" (VCCR) is "supplie[d]" to the C6SRAM "memory," Appx111(14:8-11), as claim 9 requires.

When the processor enters "deep sleep" (what Intel calls "PackageC7"), VCCR falls below RING_RETENTION_VOLTAGE as it is gradually reduced to zero. Appx2667-2670. Conte explained that, in that state, "the mux is switched to supply [VCCIO] to C6SRAM" to ensure the memory has sufficient voltage to retain

data. Appx2666. Thus, "when" VCCR is reduced "below" RING_RETENTION_VOLTAGE for PackageC7 sleep, "the second regulated voltage" of VCCIO is "supplie[d]" instead, Appx111(14:11-13), again as claim 9 requires. Other Intel documents confirm Conte's testimony. Appx8830-8831; *see* Appx2665-2666 (explaining operation of "power supply mux" that enables "C6SRAM [to] retain its state when" logic circuits power down).

2. Intel disputes almost none of that. It concedes that "Intel's multiplexer switches the C6SRAM's voltage supply from VCCR to VCCIO whenever the chip enters the 'Package C7' sleep state." Intel.Br.34. That is precisely "when" VCCR is reduced "below" the minimum operating or RING_RETENTION_VOLTAGE, consistent with the claim. Appx111(14:11-13).

Intel argues that VCCIO is supplied "at times when VCCR is still at or above RING_RETENTION_VOLTAGE." Intel.Br.35. Its sole support is an engineer's assertion that the processor will "switch from VCCR over to VCCIO" before it "turn[s] that VCCR supply off." Appx1863. As Conte explained, however, VCCR is "slowly ramp[ed] down" before being turned off. Appx2671-2672. That the mux switches from VCCR to VCCIO before VCCR is fully turned off does not demonstrate that the switch happens while VCCR remains above RING_RETENTION_VOLTAGE.

Intel urges that the accused products do not "us[e]" RING_RETENTION_VOLTAGE "in determining" whether VCCR or VCCIO supplies power to C6SRAM. Intel.Br.33. Whatever Intel means by "use," the argument is "a red herring," as the district court recognized. Appx81. The claims do not require some unspecified "use" of minimum operating voltage. They simply require supplying a first or second regulated voltage "***when***"—*i.e.*, "at the time"—the condition is satisfied, Appx111(14:8-13) (emphasis added), which the accused devices indisputably do. To the extent Intel urges that the claims require more, the argument is waived—Intel never sought such a construction below. *Lazare Kaplan Int'l v. Photoscribe Techs.*, 628 F.3d 1359, 1376 (Fed. Cir. 2010).

The '373 patent's specification also defies Intel's argument. It explains that a "controller" selects the first regulated voltage and controls the power-supply selector. Appx102. The selector "receives VDDmem and VDDlogic [the second and first regulated voltages] and provides one of these to [the] memory array . . . ***based on information provided by the controller***"—not based on some "use" of the minimum operating voltage. Appx105(2:55-56) (emphasis added). Intel identifies nothing in the patent that requires "using" the minimum operating voltage in the switching process in a way that forecloses the jury's infringement verdict.

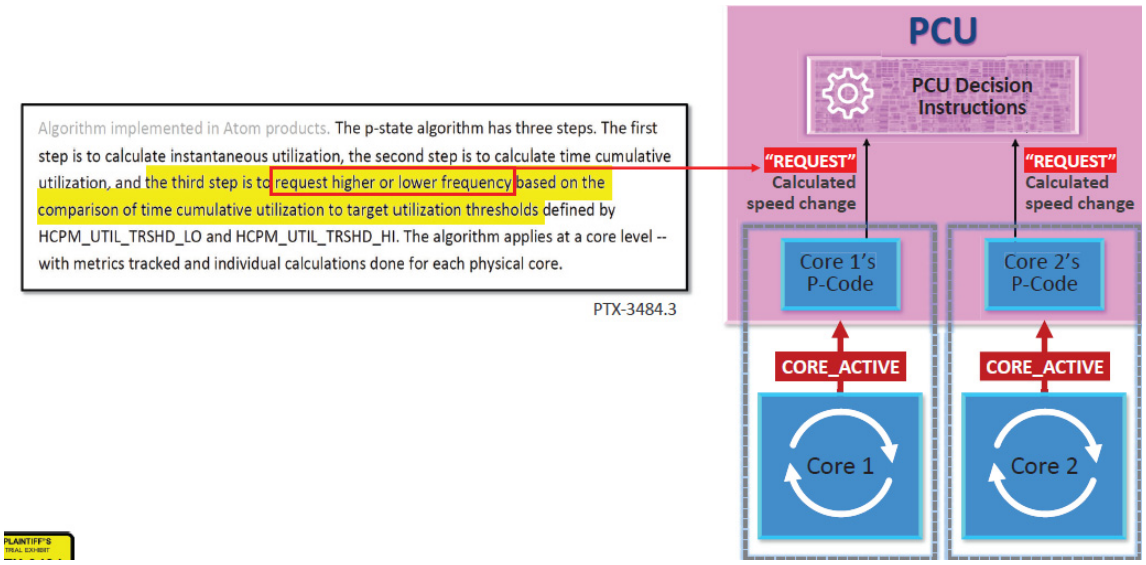
## II. THE JURY PROPERLY FOUND THAT INTEL INFRINGES THE '759 PATENT

The jury found that Intel's "Lake" processors, and their "SpeedShift" feature, infringe the '759 patent under the doctrine of equivalents. Appx10. That verdict is supported by substantial evidence. *Broadcom*, 543 F.3d at 696. Intel's argument that prosecution history estoppel bars VLSI's DOE theory is baseless.

### A. Substantial Evidence Supports the Jury's Verdict That Intel Infringes the '759 Patent Under the Doctrine of Equivalents

Infringement by DOE occurs when the accused device "perform[s] substantially the same function in substantially the same way with substantially the same results" as recited in the claims. *Ring & Pinion Serv. Inc. v. ARB Corp.*, 743 F.3d 831, 835 (Fed. Cir. 2014). The '759 patent discloses and claims a system for controlling the clock frequency in an electronic device. Appx112(Abstract). As relevant here, the claims require "a first master device" that "provide[s] a request to change a clock frequency," and a "programmable clock controller" that "receive[s] the request provided by the first master device." Appx123-124(8:50-9:4).

1. Conte explained how Intel's accused devices infringe under DOE:




Appx15183.

The recited "first master device" that "provide[s] a request to change a clock frequency," Appx123 (8:52-53), Conte explained, is satisfied by the "core" within Intel's processors working together with its P-code—a core-specific computer program located in the processor's power control unit (or "PCU"), Appx2707; Appx2697. Conte testified that when a core is active, it sends a CORE_ACTIVE signal to its P-code, which executes on a microcontroller on the PCU. Appx2691-2692; Appx2697; Appx2706. When a core's workload justifies increased frequency, the P-code "calculates a requested speed change," and sends a "request" for increased frequency, Appx2706 (quoting Appx19340-19342); Appx2709, as the claim requires, Appx123 (8:53).

Conte testified that the limitation of a "programmable clock controller" that "receive[s] the request," Appx123-124(8:59-63), is met by the "decision instructions"—a separate "module within the PCU." Appx2709; *see also* Appx2706. The decision instructions receive the request from the P-code and adjust a second core's frequency. Appx2699-2701. Based on that, Conte testified, the claims are "infringed" under DOE. Appx2709.

2. Intel argues that VLSI did not provide sufficient evidence "as to the insubstantiality of the differences between the claimed invention and the accused device." Intel.Br.42-43. Conte, however, did just that. He explained that the accused products "provide[] the same function as required by the claim, that is to provide a request," achieve "the same result as required by the claim" by "the core and its P-code sending a request to the PCU," and do so in "substantially the same way as the claim": Where the claim says "the first master device provides a request," "it's the first master device and its P-code that provides the request." Appx2707-2708; *see* Appx2704-2709. And he explained why the purported difference between the core making the request and the core and its P-code together making the request is insubstantial: "It's just an" arbitrary "difference of where an engineer draws [a] data line." Appx2707.

Intel calls that testimony "legally insufficient," Intel.Br.43, but never explains why. DOE "does not require a one-to-one correspondence between the accused

device and that disclosed in the patent." *Intel Corp. v. ITC*, 946 F.2d 821, 832 (Fed. Cir. 1991). DOE "may still apply" when, as here, "two elements of the accused device perform a single function of the patented invention." *Eagle Comtronics, Inc. v. Arrow Commc'n Lab'ys, Inc.*, 305 F.3d 1303, 1317 (Fed. Cir. 2002). Simply "relocating [a] function, ***making no change in the function performed, or the basic manner of operation, or in the result obtained***," does not defeat infringement. *Hughes Aircraft Co. v. United States*, 140 F.3d 1470, 1475 (Fed. Cir. 1998), *abrogated on other grounds by Festo Corp. v. Shoketsu Kinzoku Kogo Kabushiki Co.*, 535 U.S. 722 (2002). Intel's expert never testified that it was technically significant that the P-code was located in the PCU rather than within the core, and Intel offers no reason now.

Nor does Intel argue that the claim term "master device" ***itself*** somehow excludes a core operating in conjunction with a software module like the P-code. The specification is clear that the claimed "devices" can comprise a "combination" of "integrated circuits . . . and/or software." Appx120(2:55-56).

3. Intel argues that "Conte's equivalents theory was also nonsensical," because under it, "the ***same*** component—the PCU"—"both 'provides' and 'receives' the request." Intel.Br.43-44. As the district court found, that "misconstrues Dr. Conte's testimony." Appx87. Conte explained that, although the core P-code which (together with the core) "provides" the request, Appx2707, and the

decision instructions code which "receives" the request, are physically located in the PCU, they are separate "module[s]," Appx2709. Intel's engineer confirmed that the PCU "P-code" comprises separate "module[s]" or "component[s]." Appx2748. Intel cannot explain what is "nonsensical" about one component of the PCU sending a signal to another component of the PCU. A "reasonable jury" could "find infringement." Intel.Br.44.[3]

### B. Intel's Prosecution History Estoppel Argument Fails Because the Amendments to the "Master Device" Limitation Did Not Narrow Claim Scope

Intel's prosecution history estoppel theory (Br.37-42) fails. Prosecution history estoppel applies when "an amendment is made to secure the patent and the amendment narrows the patent's scope." *Festo*, 535 U.S. at 736. Intel invokes an amendment during prosecution replacing claims reciting "[the] at least one master device" with claims reciting "[a/the] master device." Appx8316-8317; Appx8368. According to Intel, that narrowed the "master device" limitation to require that a single component provide the claimed request, precluding infringement where "the master device" does so "in combination with another component" (the P-code). Intel.Br.40.

[3] The court held that Intel "waived" any claim construction under which "the 'first master device' and 'programmable clock controller' must always comprise entirely separate and distinct circuits." Appx87. Intel disavows any such "construction" here. Intel.Br.45.

The district court correctly found that the relevant "amendment did not narrow the claim scope." Appx53. Intel mischaracterizes the amendment to the "master device" limitation as an effort to overcome "rejections based on the Ansari reference." Intel.Br.38. ***Multiple*** limitations were amended during prosecution. Compare earlier claim 22 (depended from claim 18), Appx8316-8317, with new claim 44, Appx8368:

| | |
|---|---|
| 18. A system comprising . . . at least one master device coupled to the bus . . .<br><br>22. The system of claim 18, wherein the at least one master device provides a corresponding trigger input, wherein the trigger input includes a request to change the variable clock frequency. | 44. A system comprising . . . a master device coupled to the bus, the master device operable to provide a request to change the clock frequency of the bus in response to a predefined change in performance of the master device . . . |

***Only*** the amendments to the "request to change the clock frequency" limitation (blue) were made to overcome Ansari; the amendments to the "master device" limitation Intel invokes (yellow) were made for brevity and simplification, wholly unrelated to Ansari. *See* Appx8372-8373.

1. Ansari discloses a system with "master" and "slave" devices connected to a shared bus. Appx4479 (abstract); Appx4485 (Fig. 6). Ansari discloses a "bus arbiter" that "determines the speed of the bus" for each data-transfer transaction "by analyzing the source and destination" devices. Appx4489 (4:34-40). To communicate with a slave device, Ansari's master device "generates a request to

[the] bus arbiter indicating" the source and destination devices and "the nature of the transaction." Appx4491-4492 (8:65-9:5).

Intel argues that "[o]nly after the applicant narrowed the claims to require that 'the master device' . . . provide the 'request' to change frequency did the examiner withdraw the Ansari-based rejections." Intel.Br.39. Not so. The debate between the patentee and the examiner concerning Ansari involved the ***nature*** of the "request," ***not*** the ***component*** that sends the request. Earlier claims recited a "request to change the variable clock frequency," without limitation. Appx8316-8317 (pre-amended claims 18, 22). The examiner rejected those claims based on Ansari because Ansari disclosed the master device making a request and an arbiter receiving the request to access the bus that could result in the arbiter changing bus frequency. Appx8205; Appx8263. The patentee responded that the request sent by Ansari's master device "does not request an increase in bus frequency," but instead merely "indicat[es] the nature of the [bus] transaction" when seeking to access the bus. Appx8241-8242. The patentee argued that the "bus arbiter" determines the increase in clock frequency based on the transaction type. *Id.* The examiner, however, again rejected the claims. Appx8343-8344; Appx8348-8349.

The patentee overcame that rejection by replacing the claims with new claims reciting an ***additional limitation***—"provid[ing] a request to change the clock frequency of the bus ***in response to a predefined change in performance of the master***

***device***." Appx8368 (new claim 44) (emphasis added). While that amendment limits the ***characteristics*** of the claimed "***request***," it has nothing to do with Intel's prosecution history estoppel argument, which concerns ***which component(s)*** in the system provide the request.

Intel's argument that Ansari discloses a "request . . . performed by two components" rather than one, Intel.Br.38, was never raised in Intel's post-trial briefing; it is waived. It also fails. In Ansari, as in the '759 patent, a master device generates a request. *Compare* Appx4493 (11:4-14) ("master 624, generates a request to bus arbiter 628 to gain control of bus 620 for a transaction"), *with* Appx123 ("master device . . . provide[s] a request to change clock frequency"). The second "component[ ]" Intel cites—Ansari's "arbiter"—does not generate the request. Instead, Ansari's arbiter ***receives*** the request and uses it to "change the frequency," as Intel's cites show. Intel.Br.38 (citing Appx8257). Contrary to Intel's suggestion, none of the rejections involving Ansari concerned the ***number of components*** involved in generating the request. Indeed, the examiner argued that Ansari's master device alone generates a request. *See* Appx8205; Appx8257; Appx8263 (examiner: "the master requesting to own the bus includes the request to increase the frequency"); Appx8298-8299; Appx8305-8306; Appx8344-8345; Appx8349.

2. The change Intel relies on—replacing "[the] at least one master device" with "[a/the] master device"—reflects a grammatical preference; it did not

narrow the claims to require that a single master device ***alone*** generate the request. *See* Intel.Br.39-40. In patent claims, "a" means "at least one." *Crystal Semiconductor Corp. v. TriTech Microelectronics Int'l, Inc.*, 246 F.3d 1336, 1347 (Fed. Cir. 2001). As the district court found, changing "at least one" to "a" does not substantively change claim scope. Appx52-53. The phrase "a master device" in the new claims is identical in meaning to "at least one master device" in the earlier claims, because "at least one" and "a" are synonymous. Moreover, where "the" is used to refer back to an element introduced with "a," that element "reflects the same potential plurality." *Baldwin Graphic Sys., Inc. v. Siebert, Inc.*, 512 F.3d 1338, 1343 (Fed. Cir. 2008). Thus, "the at least one master device" in the earlier claims, and "a master device" followed by "the master device" in the new claims, have the same meaning as well.

Intel acknowledges that, to overcome that "general rule," the "context [must] ***clearly evidence[]***" a contrary meaning. Intel.Br.41-42 (emphasis added). But Intel's ***sole reason*** for its construction is its erroneous assertion that the patentee replaced "at least one master device" with "a master device" to overcome Ansari. *Id.* This case is thus wholly unlike *Tivo, Inc. v. EchoStar Commc'ns Corp.*, 516 F.3d 1290, 1303-05 (Fed. Cir. 2008), and *Philips Elecs. N. Am. Corp. v. Contec Corp.*, 177 F. App'x 981, 987 (Fed. Cir. 2006), on which Intel relies, Intel.Br.41-42.

Intel insists an intent to narrow must be presumed, because "there would have been no need to amend [the] language" otherwise. Intel.Br.42. But "the ***accused infringer***"—Intel—has the burden to "establish[ ] that the amendment was a narrowing one." *Festo Corp. v. Shoketsu Kinzoku Kogyo Kabushiki Co.*, 344 F.3d 1359, 1366 (Fed. Cir. 2003) (emphasis added). Regardless, as the court found, the amendment served to avoid the examiner objecting to grammatical "informalities" in the claims. Appx32-33; Appx53; *see* MPEP §608.01, ¶7.29. The examiner had previously found claim language "not clear" enough "to establish a relationship between the recitations." *E.g.*, Appx8196-8197. The patentee had good reason to simplify the "at least one master device/the at least one master device" language of the original claim to the "a master device/the master device" phraseology of the new claims even though it did not substantively affect claim scope.

## III. THE DISTRICT COURT PROPERLY ADMITTED THE INTEL LICENSES AS REBUTTAL

Intel complains that VLSI introduced six Intel license agreements that "were ***not comparable*** to a hypothetical license to the asserted patents." Intel.Br.46. But those agreements were not introduced to calculate damages. They responded to ***Intel's*** contention that VLSI's damages request was not "even in the same universe" of figures Intel would ***ever*** pay for patent licenses in the "real world." Appx1255. The district court acted within its discretion in admitting the licenses "as proper rebuttal." Appx17.

### A. The Intel Licenses Were Admissible Rebuttal Evidence

Intel attacked VLSI's damages figure as "astronomical" ***in the abstract***—without reference to the patents' technical merit or the sales volume Intel devices that infringed. Appx2610. Intel told the jury, "[Y]ou'll see [Intel's] licenses . . . and you can decide ***which universe*** those licenses reside in." Appx1255 (emphasis added). When cross-examining VLSI's damages expert, Dr. Sullivan, Intel claimed it would "put [his] numbers in context." Appx1699. Over objection, Intel urged that the "Texas Rangers were sold . . . for $593 million," and VLSI's "damages number would be enough to" purchase that team. Appx1699-1700. The "Dallas Mavericks . . . were sold . . . for $1.5 billion." *Id.* Sullivan, Intel emphasized, had called "$2 billion" for "the Los Angeles Clippers . . . astronomical." Appx1700-1701.

Intel's expert, Mr. Huston, purported to show the "real-world," "going rate" for patent licenses. Appx2780. He presented 20 agreements for "microprocessor patents," Appx2776, where Intel paid "from $ royalty to as much as $ royalty," Appx2777. The message was clear: VLSI's damages reflected the rarefied "universe" of professional sports franchises; in the "real world" of patent licenses, Intel would never agree to more than $ royalty .

1. The court did not abuse its "broad discretion," *Rodriguez v. Olin Corp.*, 780 F.2d 491, 494 (5th Cir. 1986), in admitting Intel licenses showing that VLSI's damages are solidly within the "universe" of what Intel pays in the "real

world" for microprocessor patents. When cross-examined regarding Intel's "compar[isons] . . . to the price tag for some sports franchises," Huston conceded that "Intel has paid more than double the price of the Texas Rangers . . . to license patents" from NVIDIA. Appx2802. And although Huston had urged that the "going rate" for "microprocessor" patents was "$ royalty " or less, Appx2777-2780, he also conceded that Intel paid $ royalty to license patents on "hyperthreading," a feature Intel touted as used in "Intel's processors," Appx2801.

With Intel having taken "great liberty" in arguing that VLSI's damages figure was not in the universe of what Intel would pay, Appx2328-2329, it was "proper rebuttal" for VLSI to debunk those arguments, Appx17-18.

2. Intel does not approach showing the licenses' "probative value is substantially outweighed by . . . unfair prejudice." *Prism Techs. LLC v. Sprint Spectrum L.P.*, 849 F.3d 1360, 1368 (Fed. Cir. 2017). Intel neither denies that the licenses rebutted its claims about a "going rate" for "microprocessor patents," nor identifies ***unfair*** prejudice in having its argument about the "universe" of patent-license rates disproven.

Intel instead argues that "noncomparable" licenses can never help juries "reliably assess damages," Intel.Br.47-48, and that these licenses did not rebut its expert's damages calculations, Intel.Br.50. But VLSI never used those licenses to calculate damages. Sullivan, who presented VLSI's damages evidence, did ***not***

testify regarding the licenses or factor them into his calculation ***in any way***. Appx1588-1674. Nor did VLSI's counsel argue for damages based on them. Appx2800.

VLSI's expert, Mr. Chandler, discussed the licenses to rebut Intel's contention that there is "some sort of a cap on the amount that Intel will pay." Appx2803; *see* Appx2805-2806. While Intel notes the need for license-comparability in "***determining***" the "***reasonable royalty***," *Elbit Sys. Land and C4I Ltd. v. Hughes Network Sys., LLC*, 927 F.3d 1292, 1300 (Fed. Cir. 2019) (emphases added), none of its cases preclude using such licenses to rebut the theories Intel pressed here.

Intel effectively argues that it can both mislead the jury ***and*** prevent VLSI from introducing rebuttal facts. Intel.Br.49-50. This Court has never gone that far. Such a "*per se* rule[ ]" would encroach on the district court's "broad discretion" over trial. *Prism*, 849 F.3d at 1368. By invoking non-comparable sports-franchise acquisitions to argue that VLSI's damages were not in the "universe" of "real-world" patent licenses, Intel invited introduction of "real-world" Intel royalty payments for ***microprocessor patents*** in that "universe." "Having opened the door" through its own comparisons, Intel "cannot contend that [VLSI's] counterarguments were unfair." *Silicon Graphics, Inc. v. ATI Techs, Inc.*, 607 F.3d 784, 799 (Fed. Cir. 2010).

That is no "post-trial rationalization." Intel.Br.49. Intel raised those comparisons long before Huston testified, when cross-examining VLSI's expert. *See* p. 45, *supra*. The court admitted the licenses based on the "great liberty" granted Intel during cross-examination. Appx2328. Its decision was clearly "premised" on the licenses "being 'proper rebuttal.'" Intel.Br.49 (quoting Appx17-18).

3. Intel's claims of unfair prejudice ring hollow. That VLSI's expert Chandler identified the Intel licenses as "***not comparable***," Intel.Br.46-47 (citing Appx2513; Appx2516-2517), underscores the absence of prejudice: The jury was instructed to consider only agreements that were "sufficiently comparable" when determining a "reasonable royalty." Appx2549. Intel cannot demonstrate an "'overwhelming probability that the jury [was] unable to follow the court's instruction.'" *United States v. Moparty*, 11 F.4th 280, 292 (5th Cir. 2021).

Although Intel derides the court's conclusion that Chandler "was not offering 'an opinion regarding a specific dollar amount of damages,'" Intel.Br.51, it is true. Chandler testified it was ***not*** his "role" to "come up with a [damages] number" in this case. Appx2514; Appx2498. None of Intel's cites supports its assertion that Chandler "suggest[ed] that Intel should pay similar amounts here." Intel.Br.51.

Intel speculates that the "jury apparently relied on the two largest" licenses. Intel.Br.53. But the jury's $1.5 billion verdict for the '373 patent is close to VLSI's requested $1.6 billion. Appx3474. And while Intel asserts that the NVIDIA

agreement is the "only . . . place in the record" where $1.5 billion appears, ***Intel*** first introduced that number as the price of the Dallas Mavericks. Appx1700.

Intel concedes that the jury's $675 million verdict for the '759 patent does not correspond to any record Intel license. Intel.Br.53. Intel's accusation that VLSI "suggested" that "the jury" consult the "New York Times" mischaracterizes the record. *Id.* VLSI's counsel noted that the "MicroUnity situation was published in the New York Times" only to respond to Intel's ***confidentiality*** objection. Appx2622.

Nor did Chandler suggest Intel will "underpay" absent "litigation." Intel.Br.51. Rather, he explained differences between "real world" negotiations, where a party can refuse to deal, and "hypothetical negotiations" for assessing damages, which "assume" a "willing licensee." Appx2502. That was offered to rebut Huston's claim that, had he faced VLSI's royalties in the real world, he "would have rejected it and walked out." Appx2375. Intel argues that VLSI used the licenses to "insinuate[ ] that Intel was a serial infringer," Intel.Br.52-53, but provides no citation because VLSI insinuated no such thing.

### B. A New Trial Is Unwarranted

This Court may set aside a jury award as clearly excessive only when "the award . . . exceed[s] the 'maximum amount calculable from the evidence.'" *i4i Ltd. v. Microsoft Corp.*, 598 F.3d 831, 857 (Fed. Cir. 2010). Here, Sullivan's testimony

supported a ***higher amount*** than the jury awarded. *See* pp. 52-54, *infra*. *Giles v. Gen. Elec. Co.*, 245 F.3d 474, 488 (5th Cir. 2001), where the jury awarded "excessive" damages based solely on the plaintiff's "testimony [in] support [of] his contention of emotional distress," is inapposite.

Intel over-reaches in demanding a new trial on "infringement and validity." Intel.Br.54. Even ***if*** the licenses were improperly admitted as damages evidence—they were not—the remedy would be a new damages trial. *See Uniloc USA, Inc. v. Microsoft Corp.*, 632 F.3d 1292, 1320-21 (Fed. Cir. 2011); *LaserDynamics, Inc. v. Quanta Comput., Inc.*, 694 F.3d 51, 76-78 (Fed. Cir. 2012); *VirnetX, Inc. v. Cisco Sys., Inc.*, 767 F.3d 1308, 1326-28 (Fed. Cir. 2014). Intel cites no case where this Court overturned infringement or invalidity verdicts based on evidentiary error concerning damages. Intel's assertion that the licenses "undoubtedly infected" the jury's findings on wholly unrelated questions, Intel.Br.54, is baseless.

## IV. THE DAMAGES AWARD REFLECTS THE INCREMENTAL VALUE ADDED BY VLSI'S PATENTS TO NEARLY ONE BILLION INFRINGING UNITS

VLSI's experts satisfied the "essential requirement" for patent damages: As this Court directs, they calculated a "reasonable royalty . . . based on the incremental value" the '373 and '759 patents "add[]" to Intel's accused processors. *Ericsson, Inc. v. D-Link Sys., Inc.*, 773 F.3d 1201, 1226 (Fed. Cir. 2014). The district court did not abuse its discretion in rejecting Intel's challenges. *See Summit 6, LLC v.*

*Samsung Elecs. Co.*, 802 F.3d 1283, 1298-99 (Fed. Cir. 2015). And Intel's assertion that VLSI is entitled to "no damages," Intel.Br.55, defies the Patent Act.[4]

### A. VLSI's Damages Methodology Was Admissible

VLSI's reasonable royalty methodology involved four steps.

Step 1. VLSI calculated the ***incremental technical benefit*** resulting from Intel's infringement. Appx1525-1587; Appx2681-2683; Appx2720-2725; Appx19452-19474. Dr. Annavaram used Intel-created workloads in Intel's Power Models to calculate that the '373 patent yields a 5.45% power-savings benefit. Appx1529-1539. He separately ran benchmark tests on six laptops to confirm the workloads' real-world applicability. Appx1555; Appx3136-3142(¶¶78-93).

Dr. Conte calculated that the '759 patent provides a 1.11% performance benefit based on Intel's tests of SpeedShift's benefits, apportioned down to reflect the contribution of the '759 patent. Appx2718-2725. Annavaram relied on Intel's proprietary Fox2, a simulator Intel engineers validated as having a "perfect correlation . . . [with] Silicon." Appx3134(¶65).

Step 2. Dr. Sullivan calculated the ***economic value*** of those incremental technical benefits. Appx1588-1753. Conte explained (and it is unchallenged here)

[4] Section 284 mandates that "in no event" shall "less than a reasonable royalty" be awarded for infringement. 35 U.S.C. §284. The remedy for an "[in]correct" damages theory is a damages retrial, not "zero royalty." *Apple Inc. v. Motorola, Inc.*, 757 F.3d 1286, 1328 (Fed. Cir. 2014).

that a "1 percent power savings or a 1 percent improvement in performance can be valued as a 1 percent improvement in [frequency]." Appx1607. Sullivan translated those performance benefits (in terms of frequency, or "clock speed") into economic value by examining Intel's sales data.

Intel sells myriad processor models—with different attributes, including maximum frequencies, core counts, cache-memory sizes, etc.—at different prices. Appx1608-1614; Appx3364-3379; Appx3406-3412 (¶¶147-157).

| Processor Number | Intel® Core™ i7-4770T Processor | Intel® Core™ i7-4770S Processor | Intel® Core™ i7-4770 Processor | Intel® Core™ i5-4670T Processor | Intel® Core™ i5-4670S Processor | Intel® Core™ i5-4670K Processor |
|---|---|---|---|---|---|---|
| | | | | | | UNLOCKED |
| Price (1Ku) | $303 | $303 | $303 | $213 | $213 | $242 |
| Test TDP | 45W | 65W | 84W | 45W | 65W | 84W |
| Cores/ Threads | 4/8 | 4/8 | 4/8 | 4/4 | 4/4 | 4/4 |
| CPU Base Freq (GHz) | 2.5 | 3.1 | 3.4 | 2.3 | 3.1 | 3.4 |
| Max Turbo Freq (GHz) | 3.7 | 3.9 | 3.9 | 3.3 | 3.8 | 3.8 |
| DDR3 (MHz) | 1333/1600 | 1333/1600 | 1333/1600 | 1333/1600 | 1333/1600 | 1333/1600 |
| L3 Cache | 8MB | 8MB | 8MB | 6MB | 6MB | 6MB |

Appx19436-19438. To "isolate" the impact of increased speed on price, Sullivan used "regression analysis" to "control for other differences," yielding a clock speed "coefficient" of 0.764—meaning that "a 1 percent improvement in clock speed . . . results in a price that is 0.764 percent greater," "***separate and apart from***" other, non-accused factors. Appx1609-1614; *see* Appx1745-1747; Appx2099; Appx19327-19337.

Step 3. Sullivan multiplied the patents' incremental technical benefits (Step 1) by his quantification of economic value (*i.e.*, speed-price conversion) (Step 2) by the "revenue associated with the infringing products," to yield "[the]

additional revenues that are resulting from use of [VLSI's] technology." Appx1656-1657; *see* Appx1654-1664. He calculated that, based on sales volume infringing units, Appx1654, Intel made an additional $2,115,862,744 in incremental revenues from the '373 patent, and an additional $1,048,541,661 from the '759 patent. Appx3446-3448 (¶¶219-233).

Step 4. To calculate a reasonable royalty, Sullivan focused on the "portion of the realizable profit" attributable to the patents. Appx1658-1670; Appx3461-3465 (¶¶295-313).

First, Sullivan calculated incremental ***profits*** by deducting infringement-specific costs from incremental revenues. It is unchallenged here that those costs included infringement-specific sales costs, but no additional infringement-specific manufacturing costs. Appx1658-1660; Appx3449-3451 (¶¶235-238); Appx3467-3469. Second, he explained that Freescale (the patent's owner at the time of the hypothetical negotiation) and Intel would share those incremental profits by acknowledging that Freescale contributed patented technologies, and Intel commercialized them. Relying on Intel's commercialization investments—R&D, sales, marketing, etc.—Sullivan calculated that Intel would have kept 23.8% of the incremental revenue from the '373 patent and 20.7% for the '759 patent. Appx1661-1662. That calculation accounted for both the incremental-profit and contribution

apportionments, yielding a reasonable royalty of $1,611,609,964 for the '373 patent, and $831,863,261 for the '759 patent. Appx3474; Appx15315.

VLSI tied its damages model to Intel's infringement—it isolated the ***incremental technical benefits*** relative to non-infringing alternatives; the ***economic value*** of those benefits; and the resulting ***incremental revenue and profit***. That rigorous approach "'reflect[s] the value attributable to the infringing features of the product, and no more.'" *Omega Patents, LLC v. CalAmp Corp.*, 13 F.4th 1361, 1376 (Fed. Cir. 2021).

### B. Intel's Criticisms of Dr. Sullivan's Regression Analysis Are Baseless

1. Intel argues Sullivan violated "fundamental apportionment principle[s]" because his model "***included non-accused***" features, and "***did not include***" the accused features as such. Intel.Br.55. Intel misapprehends how regression analysis works.

"Multiple regression analysis is a statistical tool used to understand the relationship between" a "dependent variable" and "independent variables." D. Rubinfeld, *Reference Guide on Multiple Regression*, *in* REFERENCE MANUAL ON SCIENTIFIC EVIDENCE 305 & n.2 (Fed. Judicial Ctr. 3d ed.). It can separate out the effect of the independent variable of interest on the "dependent variable" while "'controlling for' all the other [independent variables]." *Id.* at 336.

Sullivan's regression isolated a speed-price impact factor. *See* pp. 51-53, *supra*. While Sullivan included "***non-accused features*** as the 'independent variables,'" Intel.Br.56, they were "control factors" to be ***excluded***, leaving ***just*** the impact of speed on price. Appx1613-1614; Appx15275; Appx1654-1655; Appx3414-3445(¶¶166-218). That is ***necessary for***, not inconsistent with, apportionment and proper regression analysis.

Intel faults Sullivan for not including "the accused features" in his regression analysis. Intel.Br.56. But VLSI's technical experts ***already*** isolated the accused features' technical benefits and translated them into equivalent speed benefits. Appx1605-1607. Sullivan's regression analyzed how ***speed*** impacts ***price***. *See* pp. 51-53, *supra*. As he explained, it is analogous to measuring the value of an invention that increases fuel efficiency by first quantifying the "benefits it has on fuel efficiency," and then analyzing the effect of "fuel efficiency . . . on price." Appx1745-1746. The question in the second step is how much consumers will pay for incrementally better fuel-efficiency (or incrementally higher speed), holding all else equal.

Intel faults Sullivan for including "non-accused" product sales in his regression dataset, but that data enabled the regression to analyze (as intended) the ***whole market*** for Intel's processors, and capture price impacts and consumer choices

across that market. Appx3406(¶146). Just as this Court has discussed valuing infringing features' benefits by comparing against non-infringing alternatives, Sullivan "dr[ew] a comparison between the products that have [the technology] versus those" (*i.e.*, non-infringing products) "that don't." Appx1620(:11-16). Limiting data to accused sales would prevent that. Appx3510-3511.

Sullivan applied his speed-price factor only to ***accused*** revenues and the ***accused features'*** technical benefits. Intel cannot explain how Sullivan's ***model's*** inclusion of non-accused feature ***variables*** or non-accused sales ***data*** is inconsistent with proper regression analysis. Putting "***non-accused***" next to an unexplained citation to *VirnetX*—which did not involve regression, 767 F.3d at 1326—does not somehow prove Sullivan's testimony was inadmissible, Intel.Br.56. Intel's citations to cases rejecting regressions for fact-specific reasons bearing no resemblance to this case likewise prove nothing. Intel.Br.56-57.

2. Intel's unspecified "difficulties" in using regression to "estimate the contribution of product attributes [to] prices" do not establish an abuse of discretion. Intel.Br.57. The Federal Judicial Center's Reference Manual supports using regression to value patented features, pointing to calculating the effect of "infringement" on the "price of the product" in a "patent infringement case" as an exemplary application. Rubinfeld, *supra*, at 306-07 & n.2; *see also* Appx18846-18902; Appx18952-18957. One of Intel's "experts uses regression analysis in his

own academic work to evaluate the effect of features on prices." Appx1611; *see* Appx3416-3418(¶¶170-171); Appx18904-18950.

Intel's assertion that no one has "used a regression analysis to value a patented feature outside litigation" is false and does not justify exclusion. Intel.Br.57. Regression has been so used (Appx1610-1611), but it often requires extensive "confidential information" that is unavailable "outside of [litigation]." Appx1745.

3. Intel's accusation that the district court abandoned its gatekeeper role, Intel.Br.56-59, lacks merit. The court heard extensive argument on Intel's *Daubert* motion. Appx4741-4772. It found that regression "is a powerful tool" for "understand[ing] the relationship between a dependent and an explanatory variable," and is "commonly used." Appx19 (quoting *United States v. Valencia*, 600 F.3d 389, 427 (5th Cir. 2010)). Intel offered only *ipse dixit* that Sullivan's "inclusion of non-accused products and features made his model unreliable." Appx19. The court did not err by deeming these arguments "properly addressed to the model's weight, not its admissibility." *Id.*

### C. VLSI's Experts Properly Quantified the Patents' Technical Benefits

Intel's contention that VLSI improperly "included" non-accused features in determining the patents' technical benefits is erroneous.

1. Annavaram calculated the '373 patent's benefits using Intel's own accused-product-specific Power Models, ***only*** for the infringing PackageC7

state. *See* p. 51, *supra*. Intel ***does not challenge*** that analysis itself. Instead, Intel states that, "[w]hen Dr. Annavaram ran tests to determine which Power Model inputs to select for his calculations," several laptops contained non-accused Intel micro-processors. Intel.Br.60. But Annavaram merely used the laptops to select ***which*** Intel-created "workload[s]" in the Models most closely matched real-world conditions. Appx3140-3143(¶¶88-96); Appx1534-1537(534:14-537:9). Annavaram's selected workload matched ***both*** accused-product and non-accused-product tests. *See* Appx1557; Appx3128-3133(¶¶51-60); Appx3141-3142(¶¶91-92); Appx1570-1572. Intel nowhere contends that this workload was unreliable, *cf.* Appx1995-2001(995:21-996:9)—only that Annavaram over-verified Intel's data.

Intel's complaint that Annavaram looked at the "CoreC7 state" in selecting a workload is immaterial for the same reason. Intel asserts that this "inflated his power calculations," but does not explain how. Intel.Br.60. Intel is incorrect. Annavaram ***never*** used the laptop data, including the objected-to CoreC7 data, as ***inputs*** to his calculations—***only*** as one of multiple conditions in selecting a workload. *E.g.*, Appx1570-1571 ("this data does not go into any computation"); Appx1560; Appx1583-1584(583:17-584:17); Appx3130-3132. Intel does not argue that Annavaram's actual calculation included any CoreC7 data, because it did not.

2. For the '759 patent, Intel urges that Annavaram "mistakenly" calculated the power usage of the "***entire*** 'ring domain' rather than just the 'ring bus'

component." Intel.Br.61. That was no mistake. The non-infringing alternative here was a version of SpeedShift that could not "var[y] the clock frequency of the Ring/Mesh bus." Appx3215(¶1251). The ring ***bus*** is part of, and operates synchronously with, the ring ***domain***, such that bus-frequency changes apply to the entire domain. Appx18085-18086; Appx3218-3219(¶1280). Indeed, it would be "unacceptable in a commercial product" to run the ring bus at a different frequency than the other ring-domain components. Appx18087; Appx2335(:14-19). Annavaram properly measured the power usage of the entire ring domain in computing the '759 patent's benefit. Appx1540-1542(540:5-542:6).

At best, Intel's quibbles go to weight, not admissibility, as the district court found. Appx19. Intel disagrees, but does not explain why Annavaram's supposed "errors" could have rendered his testimony inadmissible. Intel.Br.55.

### D. VLSI Did Not Seek "Improper Disgorgement of Intel's Profits"

VLSI did not seek "disgorgement of Intel's profits." Intel.Br.62. The argument that VLSI sought that "legally-unavailable remedy," Intel.Br.63, is waived. It is nowhere in Intel's *Daubert* motion, Appx3597-3600, and appears for the first time in one sentence of its new-trial motion, Appx4962.

Intel's waiver notwithstanding, the *Georgia-Pacific* factors governing the "'hypothetical negotiation'" involve allocating "'incremental profits'" from infringement. *Bayer Healthcare LLC v. Baxalta Inc.*, 989 F.3d 964, 984 (Fed. Cir.

2021); *see Georgia-Pacific Corp. v. U.S. Plywood Corp.*, 318 F. Supp. 1116, 1120 (S.D.N.Y. 1970). Sullivan calculated Intel's incremental profits from infringement and shared them based on Freescale and Intel's "relative contribution," resulting in Intel receiving a 23.8% share for the '373 patent and 20.7% for the '759 patent. Appx1660-1663; *see* p. 53, *supra*.

Intel argues that Sullivan allocated "100% of Intel's profits" to VLSI, Intel.Br.63, by reducing Intel's incremental revenues by its costs and assigning "***all***" the rest "to VLSI." Intel.Br.62-63. He did not. Sullivan did "two apportionments"—"one for ***costs***" to yield incremental profits, and "one for Intel's ***contributions***" to those profits. Appx1662(:12-15) (emphases added). In calculating incremental profits, Sullivan explained there were no "meaningful" infringement-specific "manufacturing costs," and minimal infringement-specific sales costs. Appx1660. Thus, the incremental revenue was nearly all incremental profit. *Id.* As Sullivan explained, "[e]ven though the technologies have significant customer benefits, they ***do not require*** additional [implementation] costs." Appx1658-1660(658:14-660:1) (emphasis added). The "20-25%" reduction Intel points to does not reflect "costs," but ***both*** cost-deduction and profit-sharing based on Intel's commercialization "contribution." Appx1662; *see* Appx3449-3453.

Intel's assertion that Sullivan's profit split is "arbitrary" and violates *Uniloc*, 632 F.3d at 1318, and *VirnetX*, 767 F.3d at 1334—is frivolous. Intel.Br.64;

Appx3597-3600. Sullivan did not use an impermissible "rule of thumb." He calculated Intel's allocation based on ***Intel's own*** accused-product-specific "financial data." Appx1662. Intel's argument that the "profit split was also factually unsupported," Intel.Br.63, fails for the same reason. Intel's argument that Sullivan was ***also*** required to show where another party had used that specific split "to negotiate a license," *id.*, has no basis in law. It goes to weight, not admissibility.

Intel complains the district court did not address its "profit-split arguments," Intel.Br.64, but the court was not required to address a "disgorgement" argument Intel raised for the first time after trial, Appx4962, nor Intel's makeweight comparison to *Uniloc* and *VirnetX*, in denying an evidentiary motion. *United States v. Hodge*, 933 F.3d 468, 476-77 (5th Cir. 2019). Intel's demand for a "remand" for further explanation lacks merit. This Court remanded in *Finalrod IP, LLC v. John Crane, Inc.*, 838 F. App'x 562, 563 (Fed. Cir. 2021), only because the district court failed to make ***any*** ruling concerning challenged portions of an expert's report.

### E. VLSI Did Not Rely on the Accused Products' Entire Market Value

Although Intel asserts that VLSI "violated the entire market value rule," Intel.Br.64, it does not contend that VLSI used "the entire market value of the accused products" as the "royalty base." *VirnetX*, 767 F.3d at 1327.

Intel urges instead that Sullivan violated the EMVR and "skewed the damages horizon for the jury" by ***mentioning*** accused revenues to explain an early apportionment step in his damages calculation. Intel.Br.64-65. But Intel's cited cases only concern experts who sought to justify damages by comparison with total revenues—they do ***not*** suggest that the EMVR is violated by merely ***mentioning*** accused revenues. *LaserDynamics*, 694 F.3d at 68; *Uniloc*, 632 F.3d at 1318. Indeed, this Court has affirmed that introduction of "$20 billion in customer end-product sales" did not warrant retrial where the patentee "never sought to justify its damages figure based on the price of the customer end products." *SynQor, Inc. v. Artesyn Techs., Inc.*, 709 F.3d 1365, 1383 (Fed. Cir. 2013).

Here, Sullivan mentioned accused revenues only as a starting point to calculate damages: *i.e.*, multiplying accused revenues by the patents' technical benefits and speed-price coefficient to calculate incremental revenues. Appx1651-1657; pp. 51-53, *supra*. His comment regarding a "small piece" of accused revenues, Intel.Br.65, was about ***apportionment***, not ***royalties***.

> [T]hese are the ***additional revenues*** that were received by Intel as a result of using the technology from the '373 patent. Thus it is a fraction—think of it in a small piece, a sliver, if you will, of the overall revenues. ***It's just the piece that is attributable to the patented technology separate and apart from the other factors and features and functionalities of the products***.

Appx1656 (emphasis added). Sullivan was entitled to explain his calculation with numbers to avoid jury confusion. But neither Sullivan nor VLSI ever mentioned

accused revenues thereafter, and never emphasized, compared results to, or justified VLSI's royalties with Intel's revenues. Appx1651-1674; Appx1588-1623. No new damages trial is warranted.

## V. THE DISTRICT COURT DID NOT ABUSE ITS DISCRETION IN DENYING INTEL'S BELATED MOTION TO AMEND, SEVER, AND STAY

Intel's argument that it should have been permitted to "amend its answer to add [a] license defense," Intel.Br.66, overlooks a key fact: Intel never asked for that defense to be adjudicated ***in this case***. Instead, Intel made the tactical decision to litigate the issue in different courts. In September 2020, Intel told the district court it ***did not have jurisdiction*** over the defense; that Intel would assert it in ***Delaware Chancery Court***; and that the district court should ***stay the trial or stay judgment*** indefinitely pending the Chancery Court's judgment. Appx3642. Intel maintained that position when, months later—weeks before trial, and after discovery's close—it filed its so-called "motion to amend." Intel did not ask the court to adjudicate the defense, but to "sever and stay it," again asserting the district court lacked authority to decide it. And when Intel ultimately lost in ***Chancery Court***—well after trial here—Intel sought an indefinite stay of judgment in this case so a ***federal court*** in Delaware could address licensing. The district court was within its discretion to reject Intel's motion as untimely, tactical, and prejudicial to VLSI.

### A. The Court Correctly Found Intel's Delay in Filing Its Motion Unjustified and Tactical

The district court properly rejected Intel's motion as untimely. Appx68. Intel's putative license defense supposedly arose in July 2020, when Goldfish (a company Intel contends is controlled by Fortress) acquired Finjan. Appx68-70. But Intel did not seek leave to raise the defense in August, when Intel concedes it had notice. Intel.Br.66-67. Instead, in September, Intel filed a "motion ***to stay*** court proceedings." Appx3001 (emphasis added). It argued that, under the terms of the Finjan settlement, the district court "***cannot decide***" the license defense, Appx3014, which can be asserted only in Delaware courts, Appx3009. Intel nowhere contends the court abused its discretion in not granting a stay.

It was not until ***November***—weeks before the scheduled trial—that Intel sought to amend. Appx3631-3644. But Intel again did ***not*** seek to raise the defense ***in this case***. Intel argued the defense had to be asserted in "the Delaware Court of Chancery." Appx3637 & n.2. Intel urged that, after amendment, the defense should be "sever[ed]" from the case and "stay[ed]." Appx3642-3643.

1. Seeking to excuse its delay, Intel urges that it could not have asserted a license defense "before the scheduling order's March 6, 2020 deadline." Intel.Br.66. But the district court did not fault Intel for failing to amend before its license defense supposedly arose. It faulted Intel's strategic decision to wait ***months*** after learning all relevant facts before seeking to amend. Appx68. "Not only did

Intel allow fact and expert discovery deadlines to pass, it also filed summary judgment and Daubert motions without ever evincing an intent to invoke its license defense." *Id.* Intel does not dispute the court's reasonable conclusion that, given its "eleventh hour" character, "Intel's late filing of its Motion resembles more of a tactic to delay trial rather than a good faith basis for adding its defense." *Id.* The court committed no abuse of discretion in denying leave to belatedly add a defense that, according to Intel, could not even be adjudicated in this case.

Far from asking the district court to address a license defense, Intel filed an action on January 11, 2021 in Delaware Chancery Court, seeking "a sweeping declaratory judgment and an order of specific performance." *Intel Corp. v. Fortress Inv. Grp., LLC*, C.A. No. 2021-0021-MTZ, 2021 WL 4470091, at *1 (Del. Ch. Sept. 30, 2021). To prove it had no remedy at law (a pre-requisite to equitable relief), Intel insisted it was "too late for Intel to assert a license defense, or take discovery in support of that defense," as some "cases have proceeded to a verdict." *Id.* at *8. But the Chancery Court recognized that had resulted from Intel "slumber[ing] on its legal rights." *Id.* Intel "had enjoyed an available legal remedy in the form of license defenses in the Infringement Action[] for several months, since . . . July 2020." *Id.* The Chancery Court declined to excuse Intel's strategic "choice not to promptly pursue those defenses." *Id.* The district court properly reached the same conclusion here, where Intel "fail[ed] to provide a good explanation" for its delay. Appx68.

Intel insists it could not timely seek relief in district court because a clause in the Finjan settlement "***required***" Intel to complete a dispute-resolution process and adjudicate the issue Delaware. Intel.Br.67. That doubly fails. First, Intel concededly ***did*** move to amend in this case on November 10, 2020, ***before*** completing that dispute-resolution process. Appx4637. Second, Intel never showed that the dispute-resolution clause governs any dispute with ***VLSI***. The clause applies only to the "Parties" to the agreement, Appx3694(§9.3), defined as "Intel" and two "Finjan" entities, Appx3685(§1.12). Intel thus confronted no ***actual*** impediment to promptly asserting its license defense here. Intel ***chose*** not to, because it wanted to try another court (which proved unsuccessful). The district court committed no error in finding that the first consideration under Rule 16(b)(4), the party's "explanation" for the delay, weighs dispositively against Intel. *Squyres v. Heico Cos.*, 782 F.3d 224, 237 (5th Cir. 2015).

2. Moreover, by repeatedly telling the district court that it could not adjudicate Intel's license defense, Appx3014; Appx3637 & n.2, Intel waived that defense, *see Johnson v. PPI Tech. Servs., L.P.*, 613 F. App'x 309, 313-14 (5th Cir. 2015); Appx18993-18994; Appx19035-19039. Further, Intel admitted that it "is not pursuing an affirmative license defense in the present litigation." Appx18984. That admission "conclusively established" the issue, because Intel never asked the court to "permit[] the admission to be withdrawn or amended." Fed. R. Civ. P. 36(b); *see*

*In re Carney*, 258 F.3d 415, 418 (5th Cir. 2001). And the relief Intel sought in its motion—a stay of judgment to litigate this defense in ***Chancery Court***—was properly rejected as moot, because the Chancery Court dismissed Intel's complaint before the district court ruled. Appx72; Appx18998-19030.

### B. The Court Correctly Denied Intel's Requested Relief as Futile

Nor did the district court err in ruling that Intel's motion to amend, sever, and stay was "futile." Appx68; *see Squyres*, 782 F.3d at 237.

1. Intel's theory is as follows: The settlement granted Intel a "license" to "***Finjan's Patents***." Appx3687-3688(§3.1) (emphasis added). "Finjan's Patents" means patents "owned or controlled" by "Finjan" within a 10-year period after the settlement. Appx3685(§1.10). Intel contends that "Finjan" includes "Affiliates," Appx3684, which includes any person that "controls or is controlled by, or is under common control with" Finjan. Appx3684(§1.2). Intel urges that, after Goldfish acquired Finjan, Appx70, VLSI's patents suddenly fell within the definition of Finjan's Patents—giving Intel a license to all of them—because VLSI and Finjan became "Affiliates" (and therefore VLSI became "Finjan") by virtue of supposedly being "under the common control of Fortress," Intel.Br.68.

The district court considered that theory, and correctly rejected it. It explained that, under Delaware law, the general rule is that "a non-party to a contract is not

bound by that contract." Appx70 (citing cases). VLSI is not a party to the Intel-Finjan Settlement and never agreed to be bound by it. *Id.*

Nor did VLSI indirectly become a party through the Finjan-Goldfish merger. For one thing, Intel's assertion that "Fortress" "acquire[d]" Finjan, Intel.Br.66, is unfounded—as the district court found, the party that executed the merger agreement is Goldfish (Fortress-managed entities were "equity financing sources" for the transaction), Appx66. Moreover, whatever the Goldfish-Fortress relationship, ***neither Goldfish nor Fortress owns VLSI***. Appx70. VLSI is owned by CF VLSI Holdings LLC, which is in turn owned by ten separate entities, which are owned by ***pension funds*** and ***third-party investors***, not ***Fortress***. *Id.* "[N]one of the parties to the" Goldfish-Finjan merger "agreement are among the entities that own" VLSI or "VLSI's parent." *Id.* Intel cannot explain how, when neither Finjan nor Fortress nor Goldfish ever owned VLSI, they could have contracted away VLSI's patent rights via a 2012 litigation settlement between Finjan and Intel. Under Delaware law, "VLSI is not bound by the Finjan license with Intel." Appx70-71.

Intel disputes none of those facts. Instead, it insists that, under some circumstances, a non-party "affiliate" of a signatory can be bound by the agreement's terms. Intel.Br.70. But in the cases Intel cites, the non-party affiliate was under a signatory's control, *In re Shorenstein Hays-Nederlander Theatres LLC Appeals*, 213 A.3d 39, 57 (Del. 2019); *MicroStrategy Inc. v. Acacia Rsch. Corp.*, No. CIV.A.

5735-VCP, 2010 WL 5550455, at *12 (Del. Ch. Dec. 30, 2010), or gained control over the signatory, *Oyster Optics, LLC v. Infinera Corp.*, 843 F. App'x 298, 300-01 (Fed. Cir. 2021). Here, the court found that VLSI and Finjan are strangers. Appx70-71. Because VLSI was never under Finjan's control, Finjan had no power to contract away VLSI's patent rights. And because VLSI never controlled Finjan, it never assumed Finjan's obligations.

The '373 and '759 patents are not "Finjan's Patents" even apart from any issue of "control." "Finjan's Patents" are defined as patents that Finjan can license "without the requirement to pay consideration to any third person (other than employees of Finjan)." Appx3685(§1.10); Appx3687(§3.1). Finjan could not license VLSI's patents to others without paying consideration to third persons, like NXP and VLSI's ultimate owners, which have "an interest in any licensing revenues obtained by VLSI on VLSI patents." Appx3343(¶17). That is independently dispositive.

2. Intel's assertion that the district court was "required to accept Intel's allegations" that VLSI and Finjan "'came under the common control of Fortress,'" Intel.Br.69 (citing Appx3674(¶154)), fails twice over. First, even if this were merely a pleading issue, "control" is "a legal conclusion," which courts "do not accept as true." *Vedder Software Grp. v. Ins. Servs. Office, Inc.*, 545 F. App'x 30, 32 (2d Cir. 2013). This Court rejects "conclusory" allegations of "control" where

the complaint "doesn't contain 'specific facts with respect to how'" the alleged "control occurs." *Celgene Corp. v. Mylan Pharms. Inc.*, 17 F.4th 1111, 1129 (Fed. Cir. 2021). Here, Intel offered only the naked legal conclusion that "VLSI and the Finjan parties came under the common control of Fortress," Appx3674(¶154), without "specific facts" about how the "control occurs," *Celgene*, 17 F.4th at 1129.

Second, far from seeking to adjudicate a license defense ***in this case***, Intel asked the court to add that defense, "***sever***" it, and then "***stay***" judgment indefinitely pending its assertion in ***other*** courts. Appx3642-3643. Such a request for an indefinite stay is governed not by pleadings, but by "***evidence*** in the record." *VirtualAgility Inc. v. Salesforce.com, Inc.*, 759 F.3d 1307, 1315 (Fed. Cir. 2014) (emphasis added). Here, Intel's stay request rested on the theory that VLSI is (among other things) under "common control" and thus bound by the Finjan Settlement's forum-selection requirements. But Intel presented no ***evidence*** of that "control." Intel's motion to amend, sever, and stay baldly asserts that VLSI and Finjan are under Fortress' common control, Appx3638, citing only the earlier stay motion which likewise offers a conclusory allegation, accompanied by footnoted string cites and ambiguous parentheticals drawn from materials ***not*** submitted to the court. Appx3009 & nn.1-2; *see* Fed. R. App. P. 10. VLSI, by contrast, presented substantial evidence that VLSI is not bound, including evidence that Fortress neither owns nor controls VLSI. Appx18830-18843; Appx18001-18013; Appx18016-

18022. The court properly credited VLSI's undisputed evidence, finding VLSI could not "be bound by the Finjan license." Appx69-70.

The Finjan Settlement's definition of "control" requires "the power ***to direct the management and policies*** of a Person." Appx3684(§1.2) (emphasis added). Intel neither alleged facts showing nor offered evidence proving that Fortress had those powers over VLSI. *See* Appx3674(¶154). The record evidence shows that Fortress did ***not*** have power to direct VLSI's management and policies, because Fortress did "not own" VLSI, but rather "provide[d] administrative services to VLSI in Fortress's capacity as investment advisors to the owners of the company." Appx70. Intel thus failed to show VLSI was subject to the Finjan Settlement, and the district court properly concluded that "allowing Intel to amend to add a defense of license would be futile." Appx71.

### C. The Court Reasonably Weighed Prejudice

The district court reasonably held that the final Rule 16(b)(4) factor, the "potential prejudice in allowing" amendment, *Squyres*, 782 F.3d at 237, weighed against Intel. Intel would suffer no prejudice because Intel was not seeking to adjudicate the license defense in this case, and its license defense was futile. Appx71. If Intel wanted to pursue its baseless theory anyway, "it has a remedy outside of this litigation as it can pursue . . . a breach of contract claim against Finjan." *Id.* While Intel complains that the court did not "consider[]" Finjan's ability to pay any

judgment, Intel.Br.71-72, Intel never argued below that Finjan is unable to pay. The issue is thus "'waived . . . on appeal.'" *Def. Distributed v. Grewal*, 971 F.3d 485, 496 (5th Cir. 2020).

Contrary to Intel's assertions (Intel.Br.72), the court properly found prejudice to VLSI because "[t]rial . . . has already occurred." Appx72. The court did not improperly rely on its own "delay" in resolving the motion until after trial. Intel's motion urged delay: It asked the court to "sever" its "license defense" so that it could be considered ***after*** the trial, which Intel represented would "proceed as scheduled." Appx3636. On post-trial motions, after losing in Chancery Court, Intel asked the court to delay entry of judgment indefinitely and instead "wait for the decision of the federal district court in Delaware." Appx19098. The district court did not err in concluding that amendment would prejudice VLSI by "delay[ing] entry of judgment," and "prejudic[ing] VLSI's ability to license its patents to others." Appx71.

* * * * *

The district court's findings fully justify denying Intel leave to amend. Intel shows no abuse of discretion.

## CONCLUSION

The judgment should be affirmed.

November 14, 2022

Respectfully submitted,

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**FORM 31. Certificate of Confidential Material** **Form 31**
**July 2020**

# UNITED STATES COURT OF APPEALS FOR THE FEDERAL CIRCUIT

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**Short Case Caption:** VLSI Technology LLC v. Intel Corp.

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**FORM 19. Certificate of Compliance with Type-Volume Limitations** **Form 19**
**July 2020**

# UNITED STATES COURT OF APPEALS
# FOR THE FEDERAL CIRCUIT

## CERTIFICATE OF COMPLIANCE WITH TYPE-VOLUME LIMITATIONS

**Case Number:** 2022-1906

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